FLIR COMMON MODULE DESIGN MANUAL

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Night Vision and Electronics Laboratory, AMSEL-NV-SD
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FOREWORD

This document was prepared by the Orlando Division of Martin Marietta Corporation for the U.S. Army Mobility Equipment Research and Development Center, Night Vision and Electronics Laboratory (AMSEL-NV-SD), Fort Belvoir, Virginia, in response to CDRL item A021 of Contract DAAG53-75-C-0179. This document is a design manual for incorporating forward looking infrared (FLIR) common modules into night vision systems.

CONTENTS

ILLUSTRATIONS

TABLES

1.0 INTRODUCTION

1.1 General

This manual provides information for forward looking infrared (FLIR) system design using common modules. The manual provides the following:

1. Forward looking infrared system and common module descriptions;
2. Practices and procedures recommended for system specification; equipment design, and module interface;
3. Impact of module peculiarities and constraints for all affected specialty areas;
4. Procedures for alignment and setup; and
5. Module characteristics and reference material.

Equipment categories are covered from the specialist's viewpoint, although interdisciplinary constraints and overall system limitations are reflected in each equipment categroy where appropriate. The primary information for FLIR system design using the common modules is provided in section 3.0 which discusses design procedures and special system considerations. This section makes recommendations which should facilitate the specification and design of system-peculiar equipment to permit ease of integration with the common modules. The section emphasizes analytic approach, interface requirements, and the module peculiarities which affect integration. Section 2.0 provides a brief overall description of the common modules and possible system-dependent additions and options. Appendix A details the functional implementation internal to each of the 12 modules, along with

module characteristics and tolerances; Appendix B discusses video electronics noise; Appendix C and D report common module testing for vibration and electromagnetic interference; and Appendix E presents the Ratches' model for FLIR system performance.

1.2 Module Usage

Each FLIR system will be a combination of common modules and system-peculiar components. The system application and performance requirements will dictate the overall system configuration. Each system will be built around the basic set of modules (Figure 1.2-1) with system-peculiar elements added as necessary. The system-peculiar elements will normally include a front infrared (IR) afocal assembly, electrical power supply, phase shift lens, visual relay and display optics, housing, and control panel. These elements are intended to adapt to the basic set of modules to tailor the system to meet specific performance objectives. The modules then perform the functions of IR imaging, detection, electrical-to-visual signal conversion, visual collimation, and scanning. This modular approach offers performance and configuration control comparable with custom FLIR designs, but promises significantly reduced cost through reliance on common equipment.

1.3 Imaging Approach

The module approach to imaging with IR radiation is basically a parallel-channel concept. This concept is illustrated in Figure 1.3-1. The system is capable of providing up to 180 parallel detection, amplification, and display channels. Two-to-one interlace is available so that up to 360 channels may appear to be scanned for each frame. This parallel approach implies that each detector has its own preamplifier, postamplifier, and display

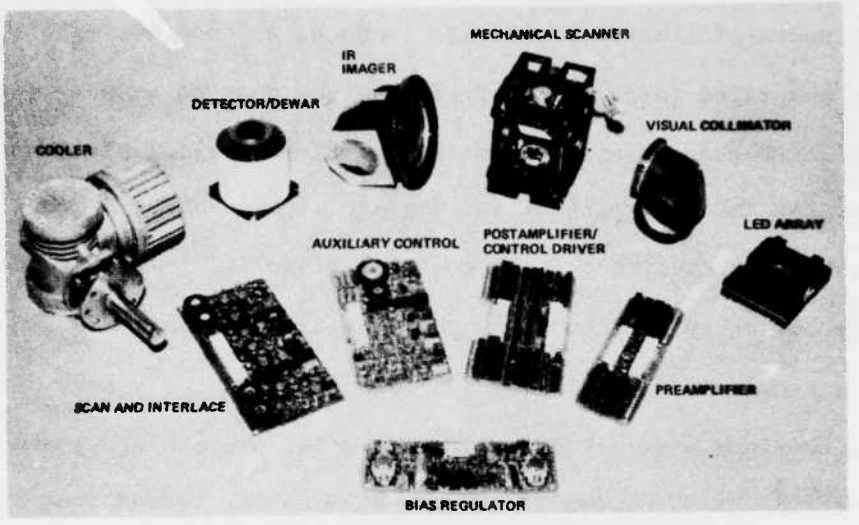


Figure 1.2-1. Common Modules (Less DC/AC Inverter Module)

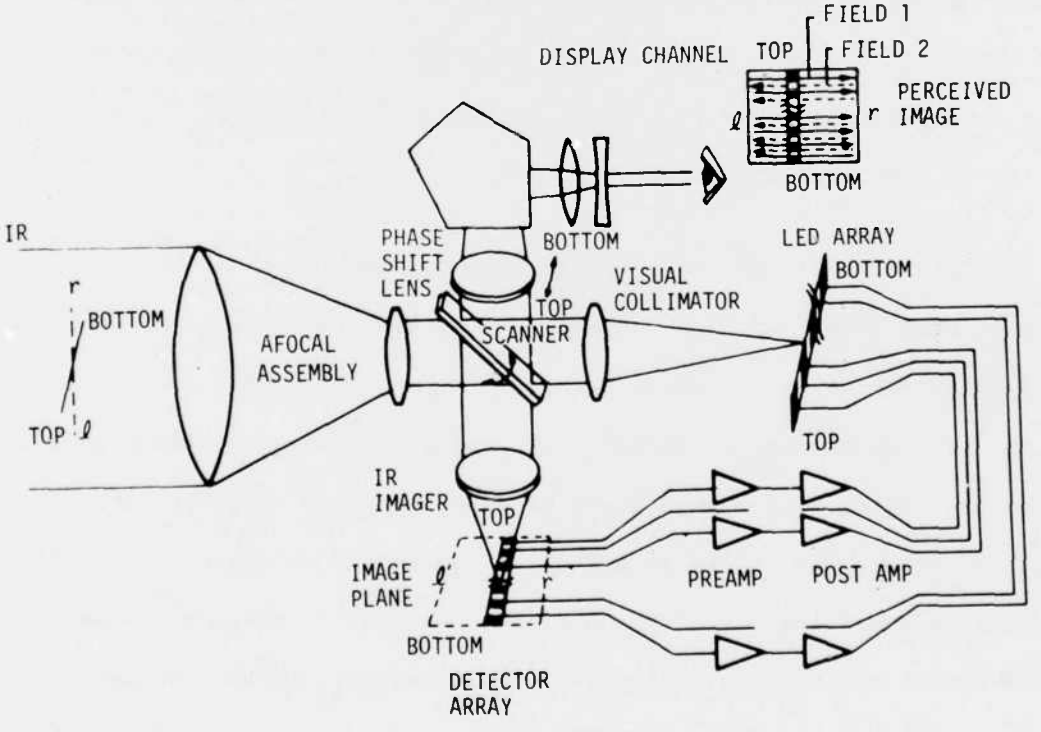


Figure 1.3-1. Parallel-Channel, Image-Forming Approach

element. Twenty such parallel channels are contained in each preamplifier module and postamplifier/control driver module, so that the modules themselves are connected in parallel to achieve the desired system resolution. Thus, a full 180-channel system consists of nine parallel electronics module sets for the preamplifier and postamplifier/control driver. The output for each channel is a light emitting diode (LED) element in an LED array. The LED array is scanned in the visual output optics so that each LED scans a single line per field. Signal output can be viewed directly through an eyepiece assembly or indirectly after processing by an image intensifier tube or TV camera. The scan rate can be varied from 20 to 60 frames per second. At the higher frame rate the LED array is scanned rapidly enough for the relatively long observer eye time decay constant to make the image appear continuous when directly viewed. Pickup by an image intensifier tube or TV camera permits biocular viewing. Remote viewing is also available when TV is used.

The parallel-channel approach has several implications for system design. First, this approach allows considerable flexibility in determining system resolution and sensitivity. System resolution can be selected in a range varying between a minimum of 20 and a maximum of 180 detection channels. (As few as five channels can be used, but each amplification module contains 20 channels.) The relatively large number of detector elements available ensures the capacity for high-sensitivity operation. Second, many signal output options are available. These options include the use of monocular and biocular assemblies and TV cameras. The output signal format from the parallel-channel approach can be serialized to a standard TV-compatible

format by using the TV camera option discussed in section 2.0. In this option, a TV camera is used as an electro-optical multiplexer. The standard format video that results is useful in applications which employ video trackers and standard TV monitors. The many options available with the basic parallel-channel module concept provide the FLIR designer considerable flexibility in configuring his system.

2.0 FLIR FUNCTIONAL DESCRIPTION

Figure 2.0-1 illustrates the FLIR functional operation to the major subsystem or module level. The figure differentiates between common modules and system-peculiar elements and notes subsystem design options by parallel flow paths. Common modules are those whose configuration is controlled by NVL:

1. Mechanical scanner (SM-D-807690-1, -2, -3)
2. Infrared imager
3. Detector/dewar (180-element and 60-element arrays)
4. Cooler (1 watt, Stirling cycle)
5. Preamplifier
6. Postamplifier/control driver
7. Bias regulator
8. Scan and interlace (30 Hz and 30 to 60 Hz modules)
9. Auxiliary control
10. Inverter (in existence, but no longer controlled by NVL)
11. Light emitting diode array
12. Visual collimator.

System-peculiar components can be added to the basic set of common modules to perform additional functions or similar functions by alternative methods.

Added system-peculiar assemblies can include:

1 Afocal optics

2 Power supply

3 Displays

4 Phase shift lens

5 Alternate cooler

6 Housing and control panel.

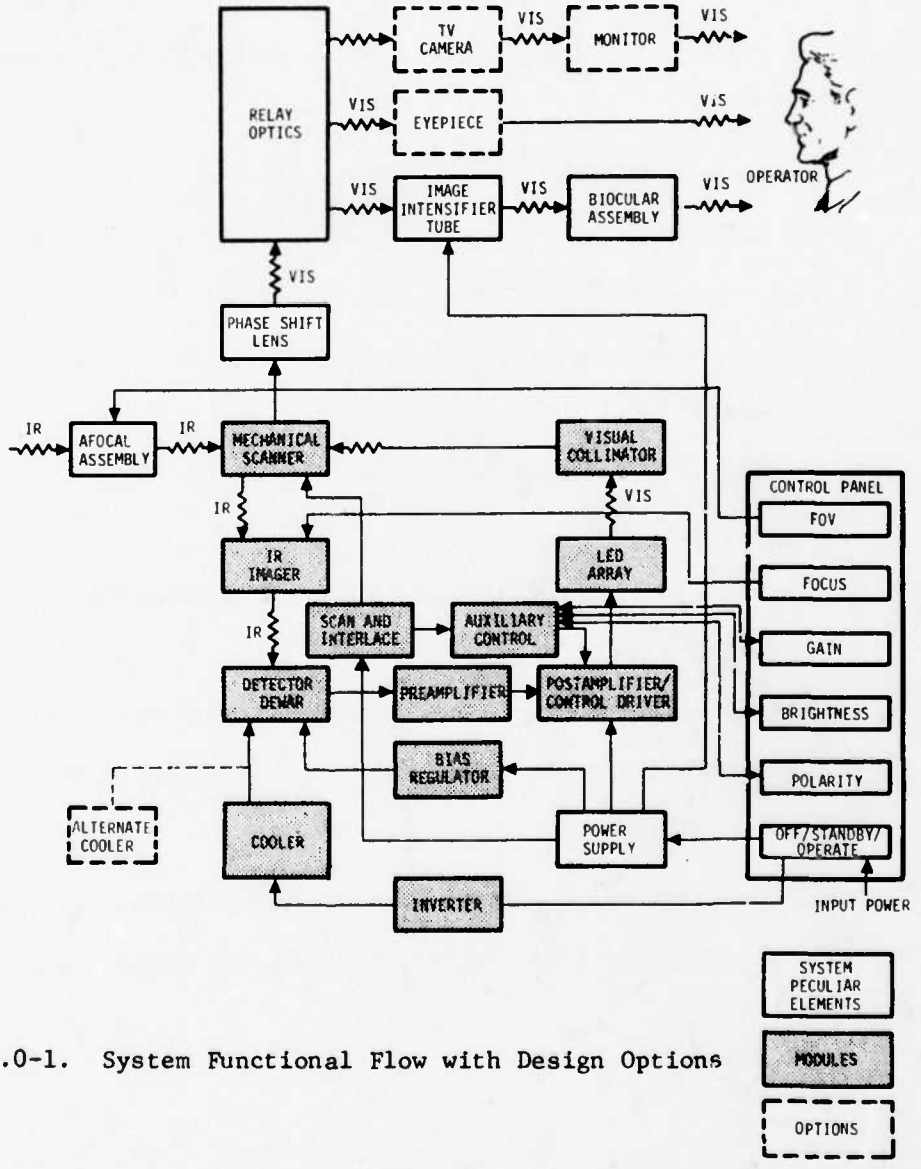


Figure 2.0-1. System Functional Flow with Design Options

A brief description of the common modules and system-peculiar elements is provided in this section to introduce assembly functions and to indicate their relative impact on a system design program. Detailed considerations for achieving an optimum system design with modules and system-peculiar elements are discussed at length in section 3.0.

2.1 Common Modules

The common modules consist of two mechanical, two optical, two signal conversion, and six electrical assemblies. The cooler and mechanical scanner modules make up the two mechanical assemblies. The optical assemblies are the IR imager and the visual collimator modules. Signal conversion is accomplished in the IR spectrum by the detector/dewar and in the visual spectrum by the LED array. The electrical modules are single curcuit boards, although up to nine preamplifier and nine postamplifier/control driver boards may be required in a system. The inverter module is contained in a separate package configuration. Brief descriptions of each module follow, and detailed descriptions are provided in Appendix A.

2.1.1 Mechanical Scanner

The mechanical scanner module is a two-axis gimbal and housing assembly. The inner gimbal is simply a two-sided, reflecting mirror that simultaneously scans IR rays across the detector array and visual rays from the LED array to form the image. This combined scanner operation is shown in Figure 1.3-1 Interlace angle and phase shift lens translations are also accomplished simultaneously when solenoids tilt the gimbal outer axis. The scanner assembly allows the system designer to choose between 30 Hz and 60 Hz scan mirror return springs. His selection will be based on the system-peculiar frame rate requirement. Adjustment of the spring positions determines mirror hor-

izontal scan angle. The gimbal outer axis has a provision for accepting and retaining the system-peculiar phase shift lens. Three variations of the scanner design are identified in drawing SM-D-807690. These options are specially configured for 60 Hz operation without a phase-shifting lens and 30 Hz or 60 Hz with a phase-shifting lens.

2.1.2 Infrared Imager

The IR optical imager module is the focusing element for the IR optical path. In a typical system application, collimated light from the afocal assembly is directed by the mechanical scanner module along the optical axis and into the aperture of this module. The module consists of three elements and a folding mirror. The first two elements are forward of the folding mirror and are movable for focus control via a motor drive or a manual mechanism. The module can function independently of an afocal assembly and, when used alone, forms an f/1.8 IR optical channel with a 2.67-inch effective focal length.

2.1.3 Detector/Dewar

The detector/dewar module performs the optical-to-electrical conversion function. A mercury-cadmium-telluride (HgCdTe) array of 180 elements sensitive in the 7.5-to-12 μm spectral region is used. This module offers the system designer the flexibility to tailor his system resolution and sensitivity. The detectors can be biased in groups of five when less than the full 180-element array is required for the system application.

The dewar provides an insulated vacuum enclosure for maintaining low detector temperature and forms a shield that limits the detector field of view (FOV) to an equivalent 75-degree cone. The detector elements must be maintained at approximately 80°K during operation.

2.1.4 Cooler

The cooler module is a miniature, closed-cycle mechanical refrigerator that operates on the Stirling cycle principle and is driven by an ac motor (117V, 400 Hz). Its function is to extract heat from the detector array in the detector/dewar module and to maintain the operating temperature of the array at a level of approximately 80°K. The detector/dewar mounts to a flange on the cooler cold finger assembly, and a flexible copper/nickel bellows and thermally conductive grease provide the thermal interface between the cold finger and the glass stem of the detector/dewar. The cooler is mounted in a system by using the threaded holes provided in either the compression head or the base drive. Heat is removed from the cooler by forced air circulation over the fins, which form an integral part of the housing and/or conduction to a mounting structure.

The cooler has a rated capacity of cooling a 1-watt resistive load to 80°K at room ambient. Although the detector/dewar presents a maximum 400 mW load, losses due to the thermal interface and elevated operating temperatures require the additional capacity inherent in the cooler design.

2.1.5 Preamplifier

The preamplifier modules perform the function of amplifying low-level signals obtained from the low-impedance photoconductive detectors. Each module contains 20 parallel amplifier channels. Preamplifier modules can be added in parallel up to a maximum of nine to handle all 180 detector channels.

2.1.6 Postamplifier/Control Driver

The postamplifier/control driver modules perform the function of amplifying the signals from a preamplifier module to a level sufficient to drive

an LED. Like preamplifier modules these also contain 20 signal channels, and additional modules may be added in parallel as required to satisfy given system requirements. The modules accept inputs necessary to control contrast, blanking, and brightness; and also provide adjustments for changing the individual gain of each channel so that overall uniformity of the system display can be adjusted at the module and/or system level.

2.1.7 Bias Regulator

The bias regulator module performs the function of supplying a low-noise, low-ripple, regulated voltage to the detectors located within the detector/dewar module. This module can drive the full 180-element array and offers ripple rejection over the complete frequency band of interest.

2.1.8 Scan and Interlace

The scan and interlace module provides the electrical signals to drive the mechanical scanner module. It provides scan mirror frequency and position control, interlace solenoid drive and phase control, mechanical failure detection, and video gate signals. The module is capable of accepting an external trigger to synchronize scanner operation with a vidicon camera. It provides all the adjustments required to modify the torque motor servo loop and solenoid drive electronics for the desired frame rate and mirror scan angle.

2.1.9 Auxiliary Control

The auxiliary control module provides an interface function between the control panel and the postamplifier/control driver module for such functions as brightness, contrast, polarity, and blanking. In addition, it provides two low-noise, low-ripple, regulated supply voltages to the postamplifier integrated circuits located within the postamplifier/control driver module.

2.1.10 Inverter

The dc/ac inverter module supplies ac power to drive the cooler module. The module converts 24 Vdc to 400 Hz, 115V and must handle high (65-watt) power levels. The unit employs a large transformer which makes it larger and heavier than the other electronic modules and necessitates a package configuration different from the single printed circuit boards of the other electronics modules.

2.1.11 Light Emitting Diode Array

The LED array module performs the function of converting an electronic signal, corresponding to the IR signal, into visible light at 6600 Å. The LED array contains 180 gallium-arsenide-phosphoride (GaAsP) diodes arranged in a format matching the IR detector array. Each element position has a corresponding detector element position. Under normal operating conditions, the LED array is driven directly from the postamplifier/control driver modules.

2.1.12 Visual Collimator

The visual collimator module collects energy from the LED array and collimates and projects it into the scanner. The module focal length is 2.67 inches. When coupled with the full 180-element array, this module provides a 15.1-degree vertical field. The horizontal field is determined by the mirror scan-angle setting.

2.2 System-Peculiar Assemblies

2.2.1 Afocal Optics

Infrared radiation is normally collected through a system-dependent afocal assembly as shown in Figures 1.3-1 and 2.0-1. This assembly performs entrance aperture definition, scene magnification, and FOV change. It is

normally equipped with mechanisms for focus control and FOV switching. The collection optics must be afocal because rays from this assembly must be collimated at the scanner module; scan of converging or diverging rays would result in a curved focal plane which would degrade off-axis. The afocal assembly is very critical to system performance and normally constitutes a significant portion of the system design effort. The assembly must provide sufficient aperture to meet the system sensitivity and resolution requirements. Successful design of the afocal optics requires attention to system trade study results, thermal effects, and narcissus.

2.2.2 Power Supply

Raw power is converted into a usable form for the common modules and other components by the power supply. Like the afocal optics assembly, the power supply is typically a major portion of the system design effort. The normal objectives of small size, low weight, and high efficiency are usually in effect, while unique FLIR considerations require special attention to achieve low line noise, low electromagnetic radiation, and good video electronics ground isolation.

2.2.3 Displays

Various display options are available to the system designer. The set of common modules provides for IR imaging, detection, amplification, and visual output by means of an LED array. The modules provide for collimation and scanning of the visible output rays. An observer would see an image if he could look directly into the scanner. However, the need for image relay, diopter adjustment, wide exit pupil, or remote viewing will normally establish a requirement for an alternative display method.

Display options, as indicated in Figure 2.0-1, include direct viewing

through a monocular eyepiece, biocular viewing of an image intensifier tube, or remote viewing through a TV camera. These and other candidate display options require hardware unique to the system application. A monocular eyepiece with the appropriate relay optics potentially requires the least amount of display hardware.

A biocular assembly is most easily implemented with the aid of an image intensifier. The use of an image intensifier tube is normally required to provide a wide exit pupil with adequate display brightness for biocular viewing. In addition, large format (approximately 40 mm) image intensifier tubes may be required to avoid limiting the resolution of the system in the display channel. Finally, a TV camera can be used to display the image on a standard TV monitor. In this option, the relay optics must be employed to focus the collimated LED rays on a TV pickup device. This option provides the capability for remote display and standard video for TV target trackers.

2.2.4 Phase Shift Lens

Compensation for electronic time lag is provided by translation of a phase shift lens. The phase shift lens is a system-dependent component that introduces slight positive power in the visual rays emerging from the collimator. This lens mounts directly on the outer gimbal of the mechanical scan module and usually consists of a single lens element. While this system component is necessary to achieve optimum image quality, it should have minimal impact on overall system design time.

2.2.5 Alternate Coolers

If system peculiarities dictate the need for power consumption, audible noise level, and/or self-induced vibration requirements that cannot be met

by the common module cooler, alternate coolers may be selected. Two possible alternates are an open-cycle Joule-Thompson cooler and a split-cycle Stirling cooler. A Joule-Thompson cooler requires no electrical power and has very low audible noise and vibration outputs, but has the disadvantage of requiring an expendable supply of clean, high pressure gas (usually nitrogen or air). A split-cycle Stirling cooler offers the packaging flexibility of a remote cold head as well as having lower noise and vibration outputs than the common module cooler. The selection of an alternate cooler depends upon system constraints and availability of a fully qualified version of the alternate selected.

2.2.6 Housing and Control Panel

A housing is required to provide a support structure for the common modules and appropriate system-peculiar elements. The control panel may mount to the housing or be remotely located. Housing structural design is a large part of the system design effort, and good results will require the normal optical and mechanical interdisciplinary dialogue. Major considerations will include thermal control, rigidity, and access. Some controls may be operated manually as a part of the opto-mechanical assemblies, or electrically from the control panel. Typical control panel functions are illustrated in the system functional diagram of Figure 2.0-1.

3.0 FLIR DESIGN PROCEDURE

This section contains procedural information to assist system designers in understanding the special requirements for incorporating the FLIR common modules into a system. Practices are recommended for system specification, equipment design, and module interface. Recommendations, module peculiarities, and special considerations for system integration are discussed. The information is provided in four sections devoted to system, optics, mechanical, and electronics design.

The system design section discusses trade studies required for establishing the major design parameters, fundamental relationships between subsystems, and performance evaluations.

The optics design section provides recommendations for IR afocal and visual channel optics design and module interface. It includes considerations for narcissus control, thermal effects analysis, and subsystem alignment. Example designs are shown.

Support structure, heat control, mounting configurations, and module interface are considered in the mechanical design section.

The electronics design section discusses overall system and module electrical characteristics. It is supported by an analysis described in Appendix B that illustrates noise computation procedures and discusses both module and total system noise characteristics. In addition, the electronics design section provides system interconnect considerations and recommendations for power supply design in the form of an example problem.

In summary, section 3.0 forms a directory of instructions for choosing undefined parameters, designing system-peculiar equipment, and integrating the equipment and modules into a complete FLIR system.

3.1 System Design

3.1.1 Approach

A baseline FLIR system configuration can be established through a tradeoff of system parameters. The tradeoff must attempt to identify the optimum set of system-peculiar design parameters consistent with performance requirements, common module characteristics, and system constraints. This section discusses an approach to system design based on the usual iterative procedure. Overall system performance requirements are discussed in terms of common performance measures. System and subsystem design requirements are related to common module characteristics and the performance measures. These design requirements result in system-peculiar component definitions and specifications. This section discusses the method for selecting undefined system parameters for use with common modules to aid in the design and optimization of the overall FLIR system.

3.1.2 Design Trade Studies and Performance Evaluation

Trade studies are conducted to determine the design values which will allow the system to meet its performance requirements. Performance requirements are generally specified by the customer for real-world operating conditions, but system performance is typically verified under laboratory conditions. Analytical performance measures are available for evaluating system performance both in the projected system operational environment and in the laboratory environment. Real-world system performance is most commonly specified in terms of range, target discrimination level, and atmospheric

conditions. However, these real-world capabilities have been related to laboratory measurable system characteristics. The latter characteristics are also commonly specified. Laboratory system performance measures include minimum resolvable temperature (MRT), noise equivalent temperature (NEΔT), and modulation transfer function (MTF). Analytical expressions that relate these performance measurements to each other and to subsystem design parameters have been developed and reported by Ratches, et al, of the Night Vision Laboratory (NVL) and by many others. The expressions are used to conduct system design trade studies and make laboratory performance predictions. Expressions and definitions provided in this section follow those of the model described in the NVL reference report. The model is described here only to the extent required to relate common module characteristics and peculiarities to the Ratches general performance model. The information, however, is intended to be sufficiently complete to permit its use in other models as well.

The system MRT is an overall performance measure for a thermal imaging system. An MRT is defined as the lowest equivalent blackbody thermal difference between a target and its background at which a spatial frequency can be resolved by an observer. The observer is assumed to have 20/20 effective vision and unlimited viewing time. The target is a four-bar, square-wave pattern with a bar aspect ratio of 7 to 1 and background temperature of 300°K.

The detailed expressions by which MRT is computed in the Ratches' model are given in Appendix E.

3.1.3 System Optical and Radiometric Relationships

The system optical and radiometric parameters are identified and related in this paragraph as an aid in accomplishing the design parameter trade

study. These relationships are provided to supplement those discussed in paragraph 3.1.2.

3.1.3.1 Infrared Optics

The more significant IR channel optical parameters include system f-number, FOV, and aperture. These parameters are related to system afocal magnification, IR imager module focal length, and detector spacing. Specifically, the IR optics effective focal length, F_e, equals:

$$F_e = F_{IR} \cdot M_a \qquad (3.1.3\text{-}1)$$

where

F_{IR} = IR imager module effective focal length (2.67 inches)

M_a = afocal magnification

$$M_a = D_a/D_e \qquad (3.1.3\text{-}2)$$

D_a = afocal entrance aperture diameter

D_e = afocal exit aperture diameter

$$D_e = D_a/M_a \qquad (3.1.3\text{-}3)$$

It follows that the system f-number, F#, is:

$$F\# = \frac{F_e}{D_a} = \frac{F_{IR} \cdot M_a}{D_a} . \qquad (3.1.3\text{-}4)$$

Note that without an afocal assembly the smallest achievable system f-number is limited in the vertical direction by the 1.75-inch scan mirror and in the horizontal direction by the 2.32-inch IR imager entrance aperture. Thus with the 2.67-inch focal length of the IR imager module, the minimum achievable f-numbers are 1.15 in the horizontal dimension and 1.53 in the vertical dimension. In a system application, the minimum achievable f-number is typically limited to no less than 1.8 to prevent vignetting when all 180 detectors are used.

The system vertical FOV, FOV_v, can be expressed by the relation:

$$FOV_v = 2 \tan^{-1}\left(\frac{d_{cc} \cdot n/2}{F_e}\right) \qquad (3.1.3\text{-}5)$$

where

d_{cc} = detector element center-to-center spacing

n = number of parallel detectors used ($\leq$ 180).

The horizontal FOV, FOV_h, can be expressed as:

$$FOV_h = M_a \cdot S_a \qquad (3.1.3\text{-}6)$$

where

S_a = mirror scan angle.

3.1.3.2 Visual Channel Optics

The major visual channel optical parameters include total system magnification and, in the case of the image intensifier tube or TV camera options, include working f-number, $F_w^{\#}$. The latter is required to compute output brightness. Visual channel optics design is discussed in section 3.2.2.3.

3.1.3.2.1 Direct View

The direct view system magnification can be expressed as:

$$M_s = \frac{F_e}{F_v} \qquad (3.1.3\text{-}7)$$

where

F_v = visual channel effective focal length

$$F_v = M_I \cdot F_{ep} \qquad (3.1.3\text{-}8)$$

$$M_I = F_{coll}/F_{rel} \qquad (3.1.3\text{-}9)$$

F_{coll} = visual collimator focal length

F_{rel} = relay optics focal length including the phase shift lens.

Thus, from equations (3.1.3-1), (3.1.3-7), (3.1.3-8), and (3.1.3-9), it follows that:

$$M_s = \frac{F_{IR} \cdot M_a \cdot F_{rel}}{F_{coll} \cdot F_{ep}} \qquad (3.1.3\text{-}10)$$

where

$$F_{ep} = \frac{\text{distance of most distinct viewing}}{\text{eyepiece magnification, } M_e} \qquad (3.1.3\text{-}11)$$

$$F_{ep} = \frac{10 \text{ inches}}{M_e} . \qquad (3.1.3\text{-}12)$$

Therefore, since $F_{IR} = F_{coll}$ in equation (3.1.3-10):

$$M_s = \frac{M_a \cdot M_e \cdot F_{rel}}{10} . \qquad (3.1.3\text{-}13)$$

3.1.3.2.2 Image Intensifier-Aided

System magnification is expressed by equation (3.1.3-13) where the eyepiece magnification, M_e, now refers to the biocular eyepiece. The output brightness of an intensifier-aided system can be computed from the relay optics working f-number, $F\#_w$, thus:

$$F\#_w = \frac{F_{rel}}{D_r} \qquad (3.1.3\text{-}14)$$

where

D_r = diameter of the relay optics aperture.

The value of D_r is defined by the visual collimator f-number to be 1.69 inches, but FOV and scan mirror vignetting considerations normally limit D_r to approximately 1.2 inches.

The power density, H, at the image intensifier is related to $F\#_w$ by:

$$I = \frac{\pi N T_o}{4 (F\#_w)^2} \text{ for aplanatic optical systems} \qquad (3.1.3\text{-}15)$$

where

I = irradiance ($W \cdot in^{-2}$)

N = effective LED radiance ($W \cdot in^{-2} \cdot sr^{-1}$)

T_ℓ = transmission of relay path.

The effective radiance from the LED array is calculated from the apparent scanned LED area under the assumption that the LED array is composed of lambertian radiators, or:

$$N = \frac{n \cdot P \cdot \varepsilon}{\pi \cdot n^2 \cdot L^2 \cdot a} = \frac{P \cdot \varepsilon}{\pi \cdot n \cdot L^2 \cdot a} \qquad (3.1.3\text{-}16)$$

where

P = LED power (W)

ε = scan efficiency (~0.75)

n = number of active channels ($\leq$ 180)

L = LED element center-to-center spacing (0.004 inch)

a = FOV aspect ratio (length/height).

Substituting equation (3.1.3-16) into (3.1.3-15):

$$I\ (W \cdot in^{-2}) = \frac{P \cdot T_\ell \cdot \varepsilon}{4 \cdot F\#_w^2 \cdot n \cdot L^2 \cdot a} \cdot \qquad (3.1.3\text{-}17)$$

The apparent brightness at the output of the image intensifier, B (fL), is:

$$B = \frac{I \cdot A(in^2) \cdot R_r \cdot G}{R_\ell \cdot A(in^2) \cdot \frac{1\ ft^2}{144\ in^2}} = 144\ (in^2 \cdot ft^2)\ \frac{R_r(A \cdot W^{-1}) \cdot G(fL \cdot fc^{-1}) \cdot I(W \cdot in^{-2})}{R_\ell(A \cdot lm^{-1})} \qquad (3.1.3\text{-}18)$$

where

A = active area of photocathode (in^2)

R_r = photocathode radiant response ($A \cdot W^{-1}$) at 0.66 μm wavelength

R_ℓ = photocathode luminous response ($A \cdot lm^{-1}$)

G = luminous gain ($fL \cdot fc^{-1}$) where $fc = lm \cdot ft^{-2}$.

3.1.3.2.3 TV Camera-Aided

The system magnification can be expressed by equation (3.1.3-13) where the eyepiece magnification, M_e, is replaced by the ratio of the TV display height, D_h, to the vidicon active photocathode height, V_h. Furthermore, the distance of distinct viewing (10 inches) is replaced by the monitor viewing distance, V_d, or:

$$M_s = \frac{M_A \cdot F_{rel} \, D_h}{V_h \cdot V_d} \quad . \qquad (3.1.3\text{-}19)$$

The signal level available for a TV camera electro-optical multiplexer can be established from the relationships previously indicated for the image intensifier-aided system. The input signal, I_s, to a TV camera preamplifier when the camera drive circuitry is in synchronism with the scan mirror, so that uniform intraframe illumination results, can be computed from the relation:

$$I_s = \frac{I \cdot A \cdot R_r}{\varepsilon} \quad . \qquad (3.1.3\text{-}20)$$

The synchronous operation of TV camera readout with LED mirror scan is recommended in applications that require the use of video trackers. Non-synchronous operation will result in abrupt intraframe signal level changes due to nonuniform illumination. The signal changes could confuse point tracker edge detection schemes and upset area tracker threshold levels. However, nonsynchronous operation, even with differing FLIR and TV camera frame rates, would not be objectionable for viewing if proper attention is given to the implementation of camera automatic gain control and the potential noise transients which occur simultaneously during FLIR dead time and active TV read time.

Table 3.1-I summarizes those parameters, for use in the above expressions, that are entirely defined by module characteristics. The values shown for D_p^* and R are minimum average specification values. The actual values may be higher. For design trade studies, the actual average values (as determined by measured data) should be used.

TABLE 3.1-I

Module Characteristics for System Design and Performance Evaluation

Parameter	Value
F_r (frames/s)	20 to 62
F_{IR} (in)	2.67
F_{coll} (in)	2.67
Ad (cm^2)	2.58×10^{-5}
n	$\leq$ 180
D_p^*, minimum average ($cm\sqrt{Hz}\cdot W^{-1}$)	$\geq 3.4 \times 10^{10}$
d_h (in)	Classified
d_v (in)	Classified
d_{cc} (in)	
l_v (in)*	0.00375
l_h (in)*	0.00075
L (LED center-to-center distance, in.)	
R, minimum average ($V\cdot W^{-1}$)	$\geq 2.0 \times 10^4$
ε	~0.75
*Per drawing SM-D-773638	

3.1.4 Trade Study Considerations

In an analysis of system requirements many system-peculiar features and system performance levels will be specified. The system features are likely to include total and instantaneous FOV, frame race, and overall angular magnification. Subsystem performance specifications will likely include MRT, MTF, and phase transfer function (PTF); and thus, indirectly, NEΔT. When the defined specifications are inserted into the system performance prediction expression, there is minimum latitude in the resultant hardware design parameters. Typically, these will include the MTF of the front IR afocal assembly in combination with the IR imager module, the MTF of the visual display channel, stabilization level, afocal aperture diameter, afocal transmittance, electronics noise magnitude, and narcissus level.

The immediate objectives of a design parameter trade study should be to:

1 Set up a system MTF budget

2 Allot a system noise budget

3 Determine an afocal aperture diameter.

The system MTF and the system noise budgets will both influence aperture diameter because aperture impacts MTF as well as signal strength. In setting up the MTF budget, care must be taken to avoid inadvertently multiplying optical component MTFs. For instance, an IR afocal assembly MTF cannot be budgeted and multiplied by the IR imager module MTF. The final system MTF budget will form the basis for specifying subsystem and component performance requirements.

A representative system noise budget is shown in Table 3.1-II. The system-dependent noise contributors are denoted by an asterisk. Noise

values shown for the common modules have been found to be typical for the 97.6 kHz electronics bandwidth. Noise values given for system-dependent sources have been shown to be achievable. All noise magnitudes are referenced to the preamplifier input.

TABLE 3.1-II

Representative System Noise Budget for 97.6 kHz Bandwidth

Source	Value (μV)
Preamplifier	0.47
Bias Regulator	0.18
Detector	∿0.84
Power Supply Ripple* through Bias Regulator	0.2
Power Supply Ripple* through Preamplifier Regulator	0.2
Postamplifier Ripple	∿0.0
EMI*	0.2
Total Root-Sum-Squared	1.04
*System-dependent contributors	

The design parameter trade study would be unlikely to include electronic bandwidth trades in imaging applications but might include them where additional signal processing, such as in video tracking or recording, is required. The MRT expression given by equation (E) in Appendix E is the system performance measure for image-forming applications. In this expression, the system electrical noise equivalent bandwidth, Δf_n, dependency in the denominator cancels with a similar, although implicit, dependency in the numerator

of NEΔT. The bandwidth dependency of NEΔT on Δf_n can be seen explicitly if NEΔT is written:

$$NE\Delta T = (n_d^2 \cdot \Delta f_d + n_e^2 \cdot \Delta f_e)^{1/2} = n_s \sqrt{\Delta f_n}$$

where

$$n_d = (NE\Delta T_{det} / \sqrt{\Delta f_d})$$

$$n_e = (NE\Delta T_{elec} / \sqrt{\Delta f_e}).$$

Because MRT dependency on Δf_n is removed, the trade study could assume an unrestricted 97.6 kHz bandpass. This dependency is removed as a result of the observer's very limited temporal response. In signal processing, however, the processing device may be capable of responding to high frequencies, and the system temporal bandpass should be optimized for the processor's requirements. This optimization can be most easily accomplished in systems that employ the TV camera electro-optical multiplexer option by adjustment of the TV camera video bandpass characteristics.

3.2 Optical Design

Recommendations for system optical integration, system-peculiar optics design, and module alignment are discussed in this section. Optical integration discussions include image orientation, scanner orientation, scan pattern, and interlace. System-peculiar optics design recommendations are discussed for an afocal optics assembly, phase shift lens, and visual channel assembly. The afocal discussion considers form, aperture stops, range focus, performance, athermalization, and narcissus. The phase shift lens discussion includes time lag compensation principles and a phase shift lens focal length derivation. An example layout is used to illustrate display

channel as well as overall optical system design considerations. Finally, system alignment and setup procedures are discussed.

3.2.1 Optical Integration

3.2.1.1 Optical Layout

Figure 3.2-1 shows a typical optical system layout. The layout shows all the optical components for the IR and visual channels.

The IR channel consists of an afocal assembly, scanner module, IR imager module, and detector/dewar module. The afocal assembly provides the required system instantaneous field of view (IFOV) through choice of afocal power. Collimated energy from the afocal is reflected by the scanner mirror into the IR imager common module. The scanner/imager combination determines the maximum entrance aperture of the afocal assembly. The IR image is formed at the detector after passing through the window of the detector/

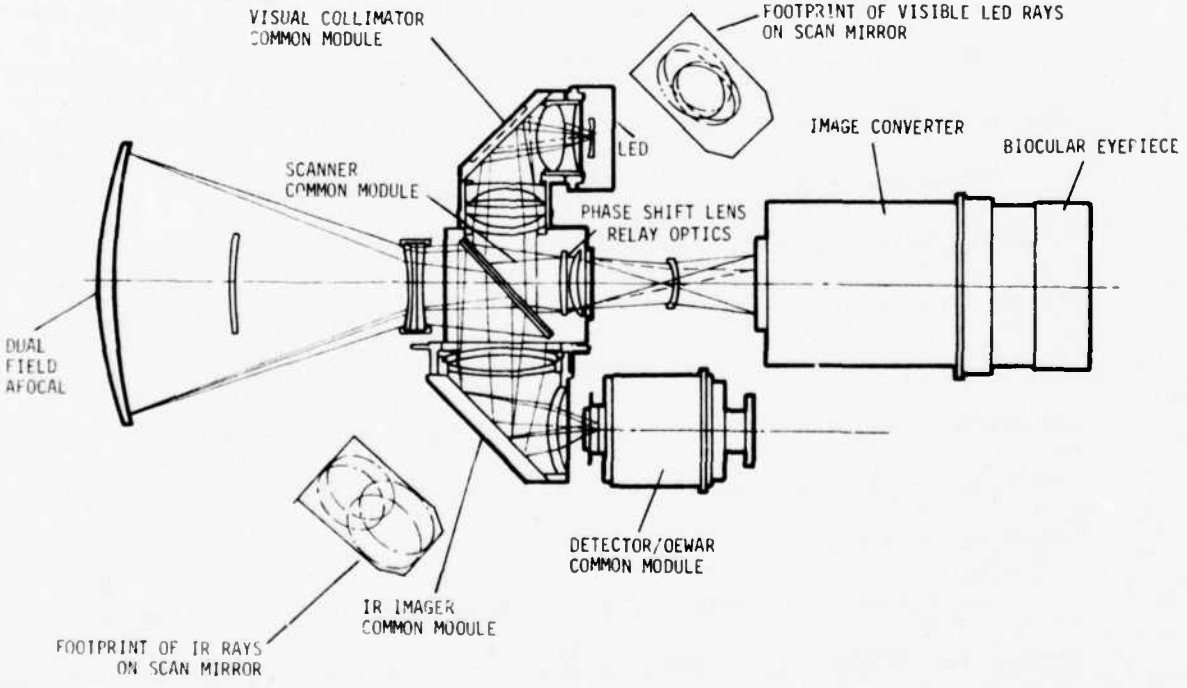


Figure 3.2-1. Optical System Layout

dewar module. Deposited on the dewar window is a dielectric filter restricting the spectrum to wavelengths between 7.5 and 11.75 μm, and a metallic filter that is sized to minimize incoming energy outside the converging cone from the IR imager.

The visual channel in this example consists of the LED module, visual collimator module, scanner module, phase shift lens, relay optics, image intensifier, and biocular eyepiece. An LED representation of detector scene information is scanned, erected, intensified, wavelength-shifted, and displayed to the operator's eyes as a magnified image of the target scene. The 0.66 μm energy emitted by the LED array is formed into a collimated bundle of rays by the visual collimator prior to entering the mechanical scanner. Upon entering the mechanical scanner assembly, the rays are scanned to form a field by the action of the scan mirror inner gimbal. At the end of each field, movement of the outer gimbal causes the scan mirror axis to rotate so that alternate fields are interlaced. After scan, the ray bundle intercepts the phase shift lens.

The phase shift lens is a positive element attached to the scan mechanism so that, with motion of the scan mirror about the interlace axis, a slight translation of this lens occurs. This translation produces an angular deflection of the (now refocusing) ray bundle of sufficient amplitude to offset the detector/amplifier-induced time lag. The angular deflection produced by the phase shift lens may be varied as required by changing the power of this element.

After passing through the phase shift lens, the converging ray bundle enters the visual relay optics assembly. These optics focus the LED imagery on the photocathode of the image intensifier tube. This tube could also be

a TV camera vidicon if a multiplexed, standard TV signal were desired. The image intensifier option permits a wide exit pupil with adequate display brightness for biocular viewing.

3.2.1.2 Image Orientation

Image orientation at the display can be controlled with the usual optical inverting and reverting devices, but module hookups and display options offer additional controls and some constraints. There is a Galilean afocal in the IR channel and an image intensifier/biocular assembly in the visual channel. Because the Galilean afocal does not invert the IR image, the object space orientation is identical to the orientation immediately in front of the scan mirror. The scan mirror then reverts the image. By a combination of reversion caused by the folding mirror and rotation associated with imaging, the right-angle IR imager effectively inverts the image at the detector plane.

In the visual channel, the LED array, visual collimator, and mechanical scanner modules must be aligned, as shown, to preserve the horizontal scan orientation. To accomplish this, the right-angle visual collimator rotates and inverts the image like the IR imager. In the example, schematic relay optics and a pentaprism transfer the resulting rotated (inverted and reverted) image to the image intensifier. The image intensifier then rotates the image to the proper orientation. Finally, the image is presented through a biocular assembly with no further inversions.

Additional flexibility for achieving proper image orientation at the display is available when a TV camera is used as an electro-optical multiplexer. Camera sweep circuitry can be set to scan any image orientation so that reconstruction at the display results in a properly oriented image.

3.2.1.3 Side or Rear Mount Configuration

The common modules allow many options for system configuration. This section outlines a procedure for general analysis of image orientation relative to the display, interlace, and optical phase shift compensation.

The analysis starts with the common module scanner where interlace and optical phase shift compensation are interrelated. Documentation on the scanner categorizes all configurations in side and rear mount modes. Figure 3.2-2 shows the visible collimator mounted on the side of the scanner, i.e., 90 degrees to the line of sight. The term rear mode is used because the visible collimator is mounted on the rear of the scanner (Figure 3.2-3), i.e., along the line of sight, opposite the afocal optics. Documentation indicates that these two basic collimator configurations require different electrical wiring. In the rear mode, drawing SM-D-773893 specifies P1-33 connected to P1-34, while side mode specifies P1-33 connected to P1-31. This wiring change alters the phase of the interlace command 180 degrees relative to the scan minor position. Since the direction of interlace is determined by the scanner module and the reference image orientation is defined by the object, between which there may exist mirrors and lenses, it is possible to configure a system that displays an inverted interlace relative to the object.

Figures 3.2-2 and -3 show some of the configuration conventions that provide the correct interlace/image relationships. The interlace can be described by either the angular displacement of the line of sight at the detector and display or the pattern of the center channel LED and detector in image and object space. Once the correct scanner interface is achieved using the conventions outlined in Figures 3.2-2 and -3, the analysis of sys-

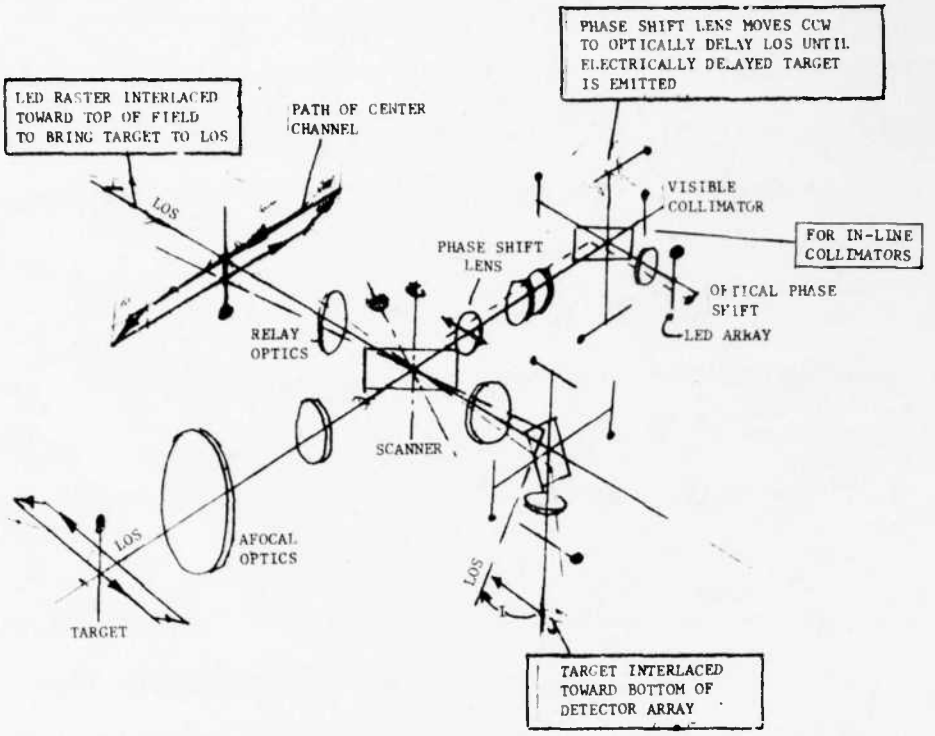


Figure 3.2-2. Rear Mount Image and Interlace Conventions

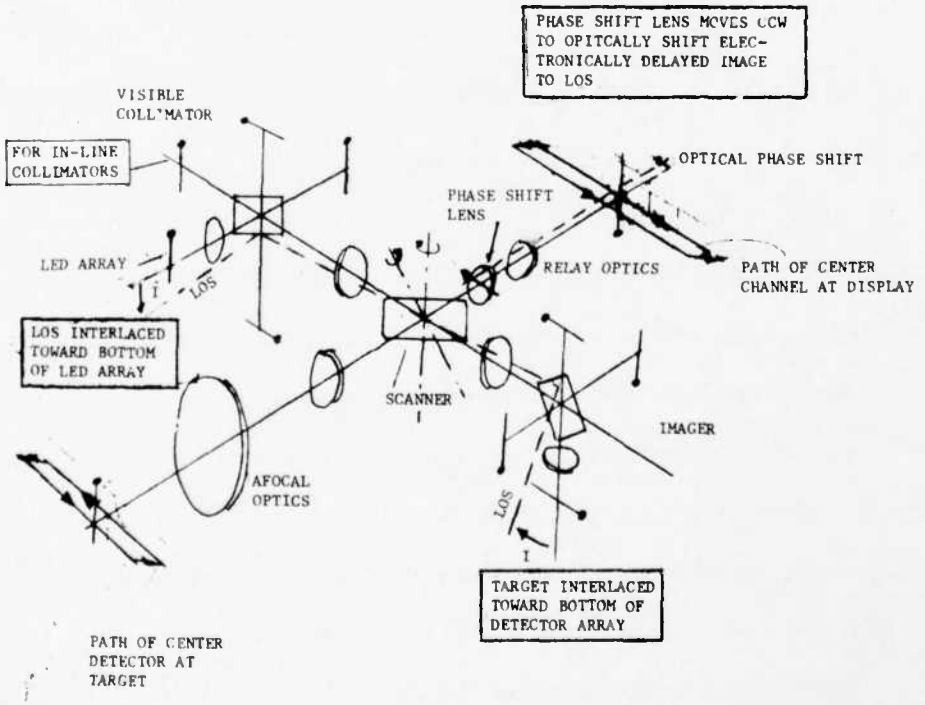


Figure 3.2-3. Side Mount Image and Interlace Conventions

tem image inversions due to additional optical elements need not include the scanner characteristics. For example, the introduction of an inverting afocal does not affect the interlace/image relationship. However, the desire to maintain an upright final image may warrant introduction of a corresponding inverting lens in the display optics.

Figure 3.2-2 defines all the required conventions for rear mount of the collimator/LED modules. These conventions were established by application of the following procedure:

1 Choose the scan direction, after interlace, as left to right at the target as viewed by the system observer.

2 Assign to the scanner the sense of angular rotation of scan gimbal consistent with scan direction as projected by the afocal optics.

3 Assign the direction of phase shift lens movement required to delay the optical line of sight until the electronically delayed signal is emitted by LED.

4 Assign the interlace gimbal sense of angular rotation to provide the required phase shift lens movement.

5 Draw an interlaced line of sight, consistent with interlace gimbal sense of rotation, to the detector and display.

6 Establish image orientation at the IR detector.

7 Draw image orientation at the display so that the LED, or FLIR raster, is interlaced to bring the target to the noninterlaced line of sight. This orientation is opposite the image orientation established at the detector for the rear mount configuration.

8 Determine the image orientation at the LED by tracing the optical inversions backward from the display. The electrical interconnect

of LED and detector must provide the optical image reference established at the detector and LED.

9 Determine the direction of scan at the display consistent with the angular sense of scan mirror gimbal and relay optics between the scanner and display.

10 Check the analysis by tracing the scan and interlace path of the center LED and detector. Verify that the paths are identical when the images at the target and display are of the same orientation.

After these steps are completed, the IR and visible optics can be modified as required for any system application in which the visible collimator/ LED module is mounted at the rear of the scanner.

The side mode conventions are shown in Figure 3.2-2. The side mode and rear mode procedures are the same except for the following changes in steps 3 and 7:

3 Assign the direction of phase shift lens movement required to optically shift the electrically delayed image to match the LOS reference at the display.

7 Draw the image orientation at the LED so that the LOS reference, defined at the display, is interlaced to match the emitted target as received by its detector. This orientation will be the same as the image orientation established at the detector for side mount configurations.

Two generalizations can be made to aid the designer who prefers to use his own convention. Both the side mount and rear mount configurations require the same phasing of the scanner and interlace gimbal. The correct wiring is rear mode, i.e., P1-33 and P1-34. This has been confirmed by

both hardware testing experience and the above analysis; however, there is one reason to retain the side-mode phasing documentation that is not related to the configuration of the collimator/LED module. Since negative lenses diverge rather than converge light, the phase shift motion using negative lenses will shift the optical line of sight in the opposite direction. The implementation of negative phase shift lenses requires side mode phasing for compensation. After the LED and detector are correctly wired and the phase shift lens/interlace phasing is correct, no optical configuration change can change the relationship of the interlace optical phase shift relative to the image.

3.2.2 System-Peculiar Optics Design

3.2.2.1 Afocal Assembly

The afocal optics can assume two forms depending on system constraints and requirements. The standard form, galilean, is the least complex, requiring as few as two optical elements. This form can be implemented with refractive or reflective optical components. The second form is an astronomical or inverting form. This form produces an intermediate image and can also be implemented with reflective or refractive optical components. The advantage of the astronomical form of afocal telescope is that it provides the largest effective aperture within a specified aperture diameter. Implementing the galilean form with reflective optical elements reduces the effective aperture due to obscuration. Implementation of the afocal optics with reflective elements reduces system weight and defocusing effects due to temperature. Also, the reflective elements of the afocal design, by definition, are free of narcissus since there can be no secondary reflections. The final choice of an afocal form depends on system objectives and constraints.

The following paragraphs discuss the design philosophy of an example galilean afocal assembly, including positioning of the aperture stop, achromatization tradeoff, performance, range focus, narcissus, and thermal effects. Also, performance of the afocal assembly when integrated with either the zinc selenide (ZnSe) imager or the TI-1173 imager is compared.

Figure 3.2-4 shows the example FLIR optical schematic with the IR optical components shaded for identification. The narrow- and wide-field afocal configurations from this schematic are shown in Figures 3.2-5 and 3.2-6. These configurations, both galilean designs, provide magnifications of 4.5 power and 1.5 power. A 6-inch germanium (Ge) primary lens is common to both magnifications. The power is changed by interchanging the narrow-field elements with the single wide-field element as shown. In the narrow field of view (NFOV), achromatization is achieved with a ZnSe and Ge lens pair. Because the wide field is only 1.5 power, it does not require achromatization.

The field is changed from 3 by 1.5 degrees to 9 by 4.5 degrees by removing the negative optical elements near the scanner and inserting a fourth optical element as shown in Figure 3.2-6. The two remaining (Ge) optical elements provide a 1.5 power galilean form.

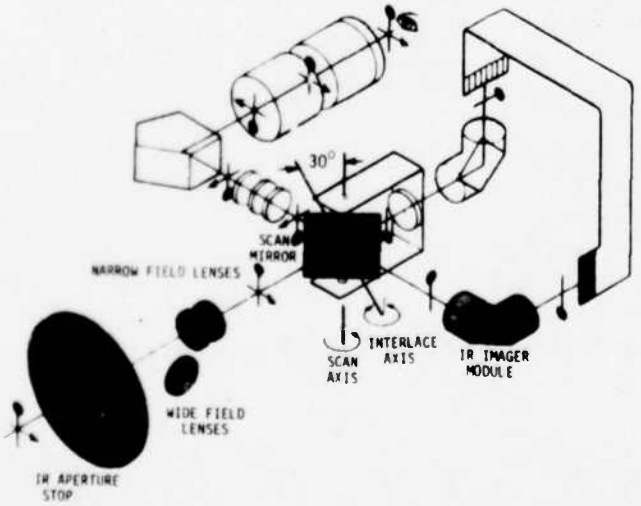


Figure 3.2-4. Optical Schematic IR Optics

3.2.2.1.1 Aperture Stop

The aperture stop for the example wide- and narrow-field afocal objective lens is selected to optimize performance within the constraints of the common modules. The effective aperture of the system is equal to the diameter of the first optical element when the aperture stop is set at the first lens as shown by the dashed line in Figure 3.2-5. Because a small percentage of vignetting causes modulation of the background by the scanner equal to signals from tactical targets, the other optical elements are large enough to eliminate vignetting of the IR energy. Ray traces verify that the optical design will not vignette the IR image for the specified field.

The wide field of view (WFOV) has a reduced aperture requirement by the ratio of the power (3 to 1) and is configured to maximize the performance of the common module FLIR to the limits imposed by the mechanical scanner and the IR imager. Maximum effective aperture is achieved when the aperture stop is placed near the scanner as shown by the dashed line in Figure 3.2-6. A mechanical aperture stop placed at this point must not

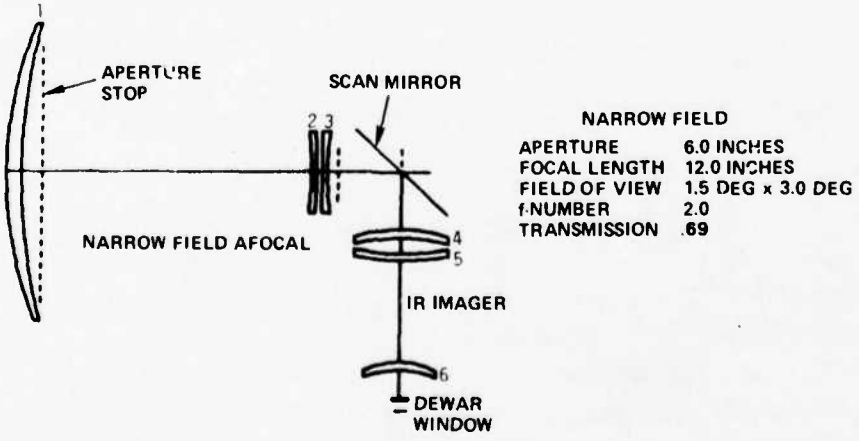


Figure 3.2-5. Example Narrow-Field Afocal Assembly

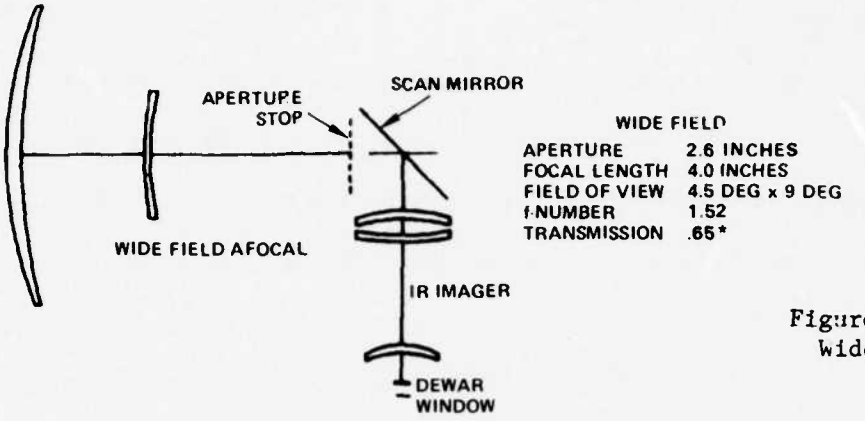


Figure 3.2-6. Example Wide-Field Afocal Assembly

vignette the full field of the NFOV optics with its stop at the first lens. Because the scan mirror is rectangular, this mechanical stop has a shape that prevents the wide-field ray bundle from missing the scan mirror while using maximum mirror surface. The shape of this stop is given in Figure 3.2-7. This technique provides the WFOV with an aperture of 2.6 inches. The stop restricts the ray bundle by flattening the circle in elevation. The loss is about 9 percent and is accounted for in the optical transmission shown in Figure 3.2-6. Computing the optical efficiency of the two fields by means of their T-numbers (NFOV-2.4; WFOV-1.88) shows that the power density in the detectors will be 60 percent greater using the WFOV. This increased power density will enhance target acquisition and detection.

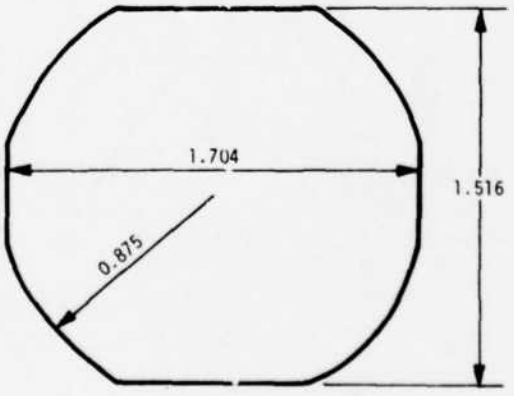


Figure 3.2-7. Wide Field of View Aperture Stop

3.2.2.1.2 Achromatization Tradeoff

This afocal design represents the optimum configuration of four- and three-element designs for cost and performance. A four-element design is required to completely achromatize any galilean afocal design. In the example system, however, a three-element configuration can meet the required modulation transfer over a 3-degree field with a 6-inch aperture. Complete axial and lateral achromatization would require two large optical elements at the entrance and two at the exit (one Ge and one ZnSe). With three elements, either axial or lateral color may be corrected, but not both. Many optical designs were studied to determine the best tradeoff between the lateral and axial chromatic errors (Figure 3.2-8). A comparison with the diffraction errors puts the tradeoff in perspective. The compromise does not significantly degrade the performance at 10 lp/mm because chromatic errors are about 1/2 of the diffraction error. The chromatic errors are about the same as the difference in diffraction error between 8 and 12 μm.

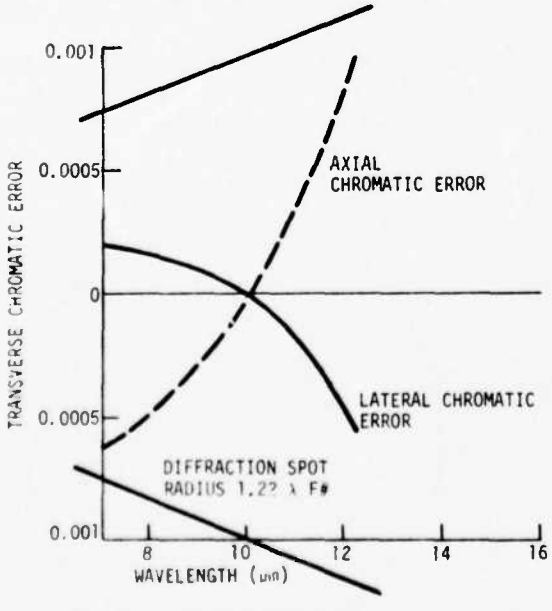


Figure 3.2-8. Lateral and Axial Chromatic Error

3.2.2.1.3 Performance

The MTF of the NFOV and WFOV afocal coupled with the mechanical scanner mirror and IR imager is shown in Tables 3.2-I and 3.2-II. The scan mirror creates an asymmetry in the field by combining the on-axis performance of the imager with the off-axis performance of the afocal assembly for points off-axis in the scan direction. Along the detector array, the off-axis performance of the imager and afocal are combined. Due to this asymmetry, the performance is not the same for points off-axis vertically and horizontally. The asymmetry requires that the afocal assembly be designed to perform well without compensation by the IR imager.

The modulation transfer in the scan direction is the parameter most basic to system performance. On-axis, the system is diffraction-limited with a modulation of 0.72 at 10 lp/mm. At half-field, 0.75 degree off-axis in the scan direction, the modulation is 0.69. This degradation, though only 3 percent, is unavoidable. It is caused by field curvature in the galilean afocal assembly. This field curvature is opposite to that of the IR imager; therefore, in the vertical field where the off-axis energy of the IR imager and afocal assembly compensate, the modulation is back to 0.72.

3.2.2.1.4 Range Focus

Range focus is achieved in the example system by increasing the spacing between lenses 1 and 2 for near targets. Range focus characteristics for the NFOV afocal assembly are shown in Figure 3.2-9 in which the separation of lenses 1 and 2 is plotted as a function of range. A minimum range of 15 meters is achieved with a 0.130-inch increase in spacing.

TABLE 3.2-I

Narrow Field-of-View Diffraction MTF

Spatial Frequency (lp/mm)	MTF (percent)		
	Axial	Full-Field Vertical	Half-Field Horizontal
Scan Direction			
2	95	95	94
4	90	89	89
6	84	84	82
8	78	78	76
10	72	72	69
12	67	67	63
14	62	61	56
16	56	56	51
18	52	51	45
20	47	47	40
Vertical Direction			
2	95	95	95
4	90	89	89
6	84	83	83
8	78	76	77
10	72	70	71
12	67	64	65
14	62	58	60
16	56	52	55
18	52	47	50
20	47	42	45

TABLE 3.2-II

Wide Field-of-View Diffraction MTF

Spatial Frequency (lp/mm)	MTF (percent)		
	Axial	Full-Field Vertical	Half-Field Horizontal
Scan Direction			
2	96	96	96
4	92	92	92
6	87	88	88
8	84	83	84
10	80	79	80
12	76	75	76
14	72	71	72
16	68	66	68
18	64	62	65
20	61	58	61
Vertical Direction			
2	96	96	95
4	91	91	90
6	87	86	85
8	82	82	78
10	78	77	75
12	73	78	70
14	69	68	65
16	65	64	61
18	61	60	56
20	57	57	52

*Vertical MTF reduced by diffraction effects from smaller vertical dimension of aperture stop

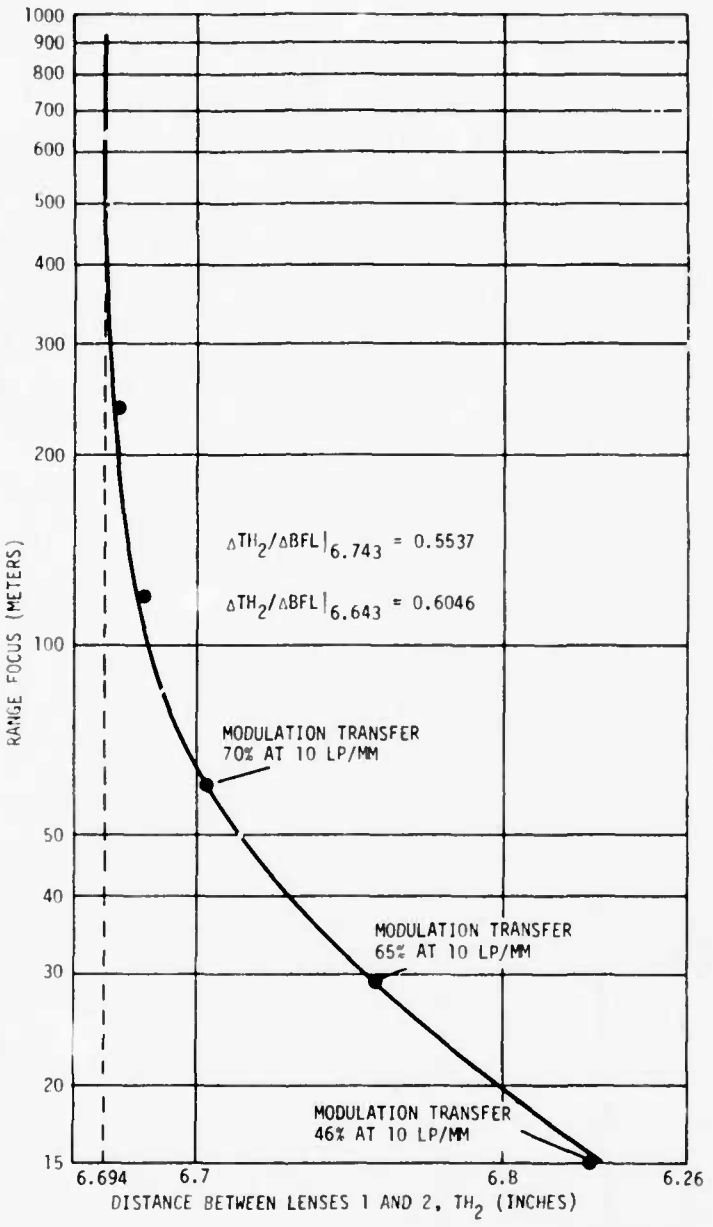


Figure 3.2-9. Range Focus Characteristics

The modulation transfer is degraded at the near ranges as the afocal assembly is modified for range focus. The sensitivity of this method for range focus is shown by the rate of change of back focal length relative to the air space between lenses 1 and 2. For a 0.010-inch change in the separation lenses 1 and 2 of the NFOV, the back focal length

changes 0.0165 inch. Because the depth of focus is 0.002 inch, the tolerance on the mechanical focus assembly must be less than 0.0012.

The advantage of range focusing with the first element is that the target will remain in focus as the field of view is switched. This can be shown from first order arguments. As the power of the afocal assembly is reduced, the change in focus with range is reduced. Correspondingly, with the change to wide field the focusing effect of the first element is reduced. The first order argument becomes clear if we choose as our reference the target as imaged by the first element. To maintain focus for both fields with targets at infinity, the negative elements of the WFOV and NFOV must collimate the target imaged by the first element. For any range, the first element is moved so that the target imaged by it is at the same point relative to the negative elements as when the target was at infinity.

3.2.2.1.5 Narcissus

In any optical system, a ghost image of the focal plane exists for every surface. Narcissus is a special effect of the ghost image from surfaces that lie between the scan mirror and the object. For the nominal scan position, these ghost images are centered on the detector. Scanning causes the ghosts to move. If a ghost is imaged near the focal plane or vignetted by the optical system, it is possible that during scan it will move completely off the detector. Because the detector will then see a 300°K ghost instead of a 77°K ghost, a signal will be generated. The signal is proportional to the intensity of the ghost.

A complete narcissus analysis to predict the magnitude and the field point of the narcissus signal was performed. The analysis showed the example NFOV afocal assembly is free of narcissus. This section presents a geometrical

analysis of a WFOV afocal assembly that does produce narcissus signals and yields a means of quantitatively calculating these signal levels. In this example, two of the four surfaces of the WFOV afocal assembly produce narcissus signals. Narcissus signals, if present, should be less than one-third of the system noise level.

Those surfaces of the WFOV afocal assembly contributing to narcissus generate signals proportional to the intensity of the ghosts. When the detector sees the ghost image of the dewar window (i.e., cold background behind dewar window), the background radiation level is reduced from the level caused by the detector seeing the ghost images of other parts of the internal hardware. The radiance from the 300°K housing, averaged over the bandpass, is 34 W/m^2-sr. At 77°K, the radiance of 7.2×10^{-5} W/m^2-sr through the dewar window from the detector plane can be neglected. The dewar window is assumed to define the effective lambertian surface of the cold background within the dewar. The difference, therefore, in background at the detector with and without a ghost image is:

$$\Delta I = \frac{\pi}{4} \frac{(N_{300} - N_{77}) \cdot t \cdot t_s}{(F^{\#})^2} \qquad (3.2\text{-}1)$$

$$\Delta I = \frac{\pi}{4} \; 34 \frac{t \cdot t_s}{(F^{\#})^2} = 26.7 \frac{t \cdot t_s}{(F^{\#})^2} \; W/m^2 \qquad (3.2\text{-}2)$$

where N = radiance

ΔI = change in image plane irradiance

$F^{\#}$ = working f-number of the narcissus system

t = optical transmission of the narcissus system

t_s = reflectance of the narcissus surface.

The change in signal, ΔS, for the average detector module responsivity of 3.8×10^4 V/W of a detector with 4×10^{-6} in^2 area is:

$$\Delta S = \frac{(26.7)\ (3.8 \times 10^4)\ (4 \times 10^{-6})}{(39.37)^2} \cdot t \cdot t_s \frac{}{(F^\#)^2} \qquad (3.2\text{-}3)$$

$$= 2.6 \times 10^{-3} \frac{t \cdot t_s}{(F^\#)^2} \text{ volts.} \qquad (3.2\text{-}4)$$

The reflectance of the narcissus surface will be less than 0.02 for a multilayer antireflection coating. The optical transmission of the narcissus system will depend on the number of optical elements between the narcissus surface and the detector. Substituting, we have:

$$\Delta S = 5.2 \times 10^{-5} \frac{t}{(F^\#)^2} \qquad (3.2\text{-}5)$$

where t is the optical transmission of the narcissus system less the factor for reflectance of the narcissus surface.

For the general case, the image of the dewar is not in focus at the detector. As the out-of-focus condition is increased, the intensity of the ghost decreases reducing the narcissus signal. The irradiance from a surface having the dimensions of the exposed cold finger, but out of the focal plane of the narcissus system, is proportional to the effective solid angle subtended at the detector. The solid angle of the narcissus system is determined by the size of the narcissus surface; if vignetting occurs, however, the true solid angle is reduced. Rays traced through the narcissus system were uniformly distributed over the narcissus surface. The ratio of rays passing to those initialized is equal to the ratio of the effective solid angle to the angle subtended by the surface. The change in signal

caused by narcissus from this surface is reduced by the ratio of rays passing to those initiated. The equation for determining the magnitude of the narcissus signal in the common module FLIR is:

$$\Delta S = (5.2 \times 10^{-5}) \frac{t}{(F^{\#})^2} \frac{\text{rays traced}}{\text{rays initiated}} \qquad (3.2\text{-}6)$$

In the geometrical analysis, rays are traced from the detector, through the optical system, to the surface under investigation, and back to the dewar window. The field point corresponding to the mirror position where the edge of the ghost image reaches the edge of the dewar window is recorded. Figure 3.2-10 shows the narcissus effect from the rear surface of the first element of the afocal with the system in the WFOV mode. The energy distribution of Figure 3.2-11 shows that the ghost starts to move off the dewar window at a 2-degree field point. Figure 3.2-12 shows the energy distribution for a field point of 3 degrees.

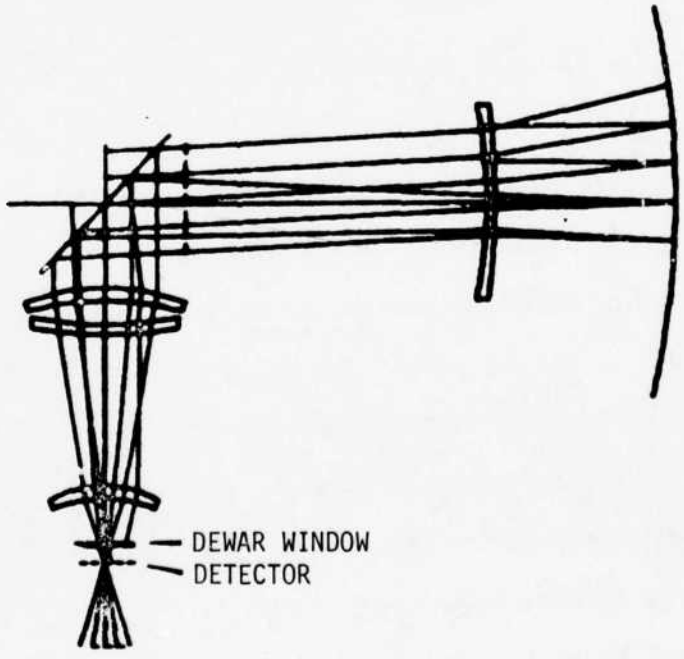


Figure 3.2-10. Narcissus System Raytrace

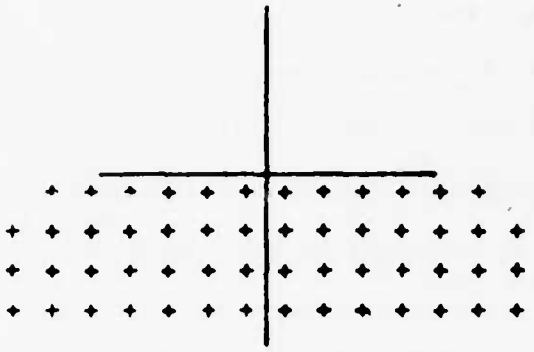


Figure 3.2-11. Ghost Image for a 2-Degree Field Point

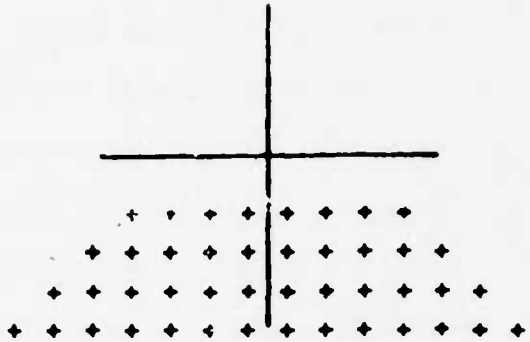


Figure 3.2-12. Ghost Image for a 3-Degree Field Point

Table 3.2-III summarizes the narcissus effects in the wide-field afocal. The effect of these signal levels on the display will depend on the gain and brightness adjustments. When targets whose signal is near the magnitude of the system noise are viewed, the effect will be maximized. The display will appear shaded in the center 4 degrees of the field for a polarity setting of white for hot targets. For very hot targets and low-gain operation, the signals given in the table will not be visible on the display.

TABLE 3.2-III

Narcissus Effects of WFOV Afocal Assembly

Surface	Signal (μV)	Field (degree)
1	<0.05	NA
2	0.41	4
3	1.04	6
4	<0.05	NA
Total Signal	1.45×10^{-6} volts	

3.2.2.1.6 Performance with TI-1173 or ZnSe Imagers

The optical design chosen for the afocal assembly meets the MTF requirements when used with either the TI-1173 imager or the redesigned ZnSe imager. Figures 3.2-13 and 3.2-14 show the performance of the two configurations over the full field. The modulation transfer for the configuration using the TI-1173 imager is slightly higher (about 3 percent) at the full-field scan point. Full-field performance is shown for verification that the afocal assembly and either imager combination will provide good imagery over the full format. Typically, full-field performance is not specified.

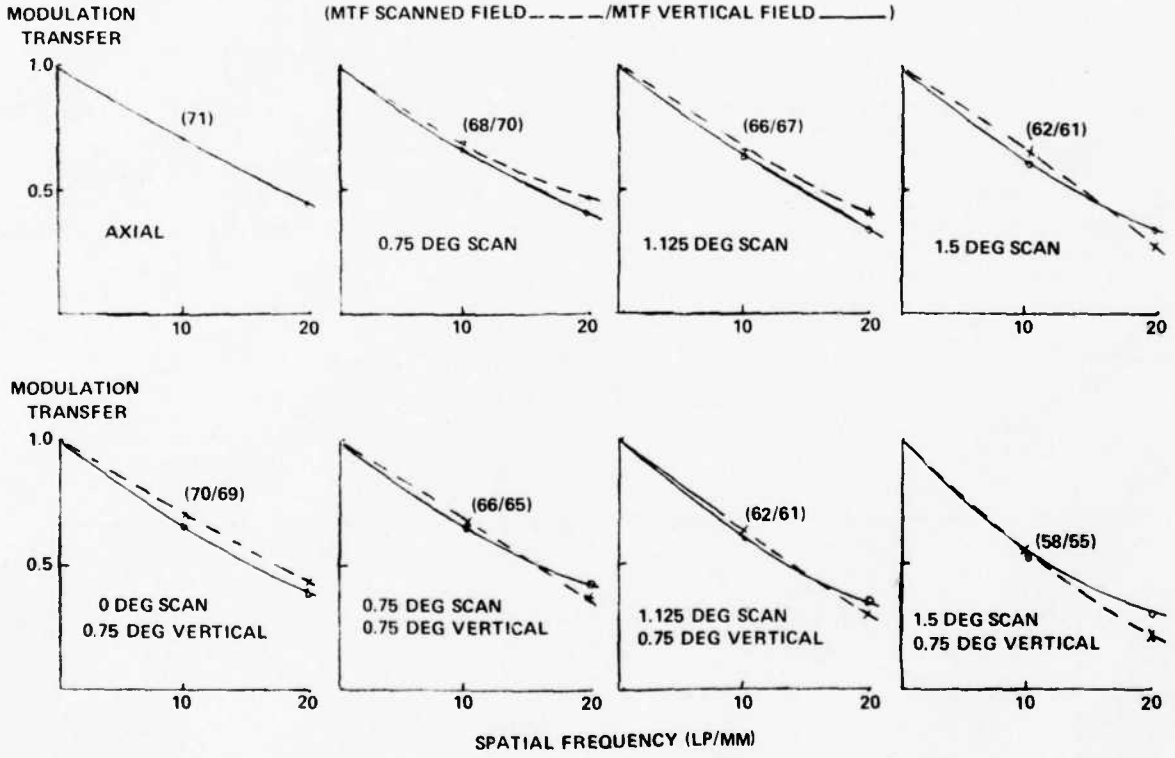


Figure 3.2-13. Afocal Assembly and TI-1173 Imager Modulation Transfer

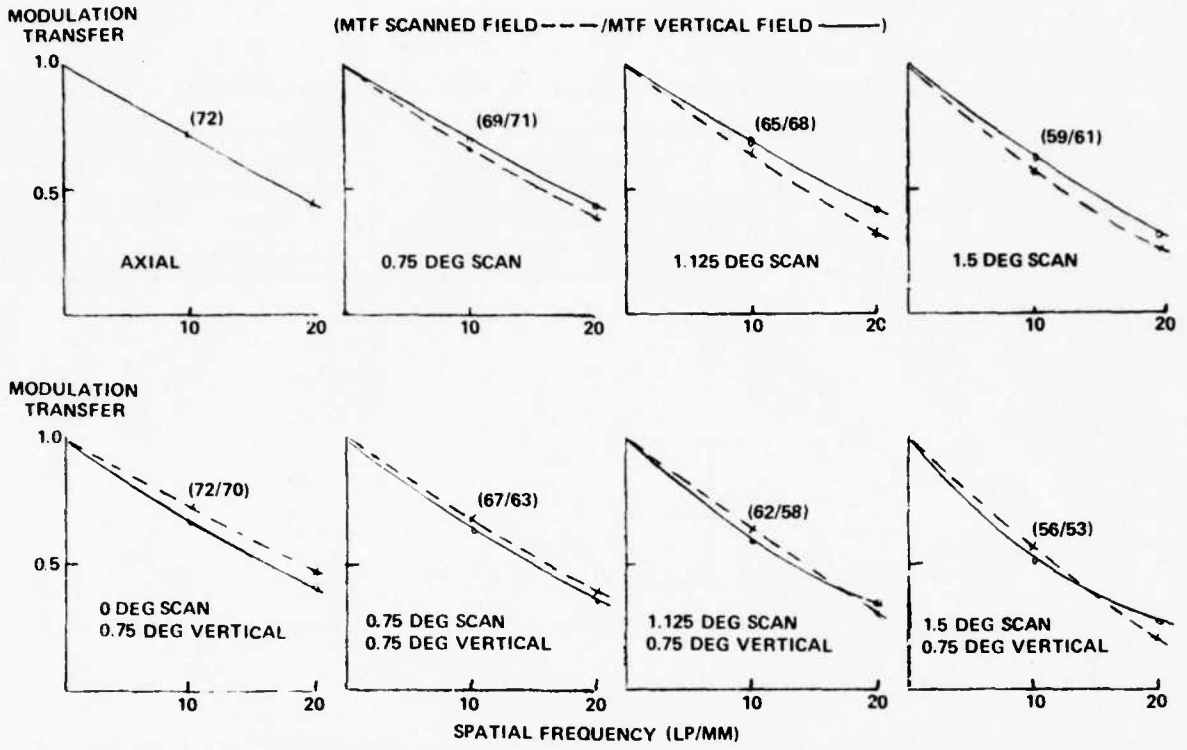


Figure 3.2-14. Afocal Assembly and Redesigned ZnSe Imager Modulation Transfer

3.2.2.1.7 Thermal Effects

A thermal analysis should be performed to determine and minimize the sensitivity of the system to temperature fluctuations. Measures of temperature sensitivity include relative focus shift and temperature tolerance. Relative focus shift refers to image plane displacement caused by changes in optical assembly temperature. Temperature tolerance refers to the maximum change in temperature that the afocal assembly can undergo, from some nominal design temperature, without degrading MTF below a design objective. Nominal design temperature is typically 23°C.

The important material considerations in minimizing system temperature sensitivity are coefficient of thermal expansion and coefficient of thermal change of index. Table 3.2-IV lists the thermal coefficients for various IR optical lenses and mounting materials.

TABLE 3.2-IV

Thermal Coefficients of IR Optical Materials

Material	Coefficient of Thermal Expansion $\Delta L/L \cdot \Delta T$ ($\times 10^{-6} {}^{\circ}C^{-1}$)	Coefficient of Thermal Change of Index $\Delta n/(n-1)\Delta T$ ($\times 10^{-6} {}^{\circ}C^{-1}$)
Germanium	$\alpha = 6.6$	$\eta = 116$
ZnSe	$\alpha = 7.7$	$\eta = 43$
TI-1173	$\alpha = 15.0$	$\eta = 49$
Aluminum	$\alpha = 23.4$	NA
Polyethylene	$\alpha = 167$	NA

Germanium, a most important lens material, exhibits large changes in refractive index with temperature.

The use of relative focus shift and temperature tolerance in an optical system thermal analysis is illustrated by the results of an analysis of the example system. These results are summarized in Figure 3.2-15. The results show that, with the optical elements at 23°C, the relative focus distance of the system is 0.259 inch. If the mechanical housing is raised to 73°C, the relative focus shifts to 0.249 inch. When the optical elements are raised to 73°C, the relative focus shifts in by 0.079 inch to a value of 0.180 inch. Now, if the first element of the NFOV afocal assembly is mechanically repositioned by 0.042 inch, the relative focus once again is 0.259 inch; however, when the afocal assembly is shifted to WFOV, the relative focus becomes 0.257 inch, off by 0.002 inch. Note from the figure that without compensation the MTF drops below 65 percent when the temperature tolerance exceeds $\pm 1.5°C$.

SYSTEM STATE	RELATIVE FOCUS (INCHES)
SYSTEM AT 23°C	0.259
HOUSING AT 73°C	0.249
REFRACTIVE INDEX FOR 73°C	0.180 (0.073)
COMPENSATION (FIRST ELEMENT – 0.042)	0.259
CHANGE TO WIDE FIELD	0.257

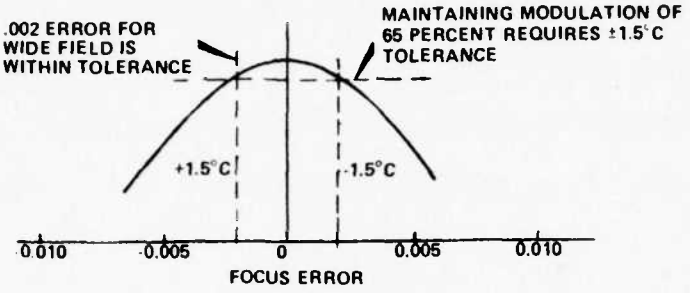


Figure 3.2-15. Thermal Analysis

3.2.2.2 Phase Shift Lens

Translation of the phase-shift lens accomplishes an apparent image advance in the direction of scan. This lens is documentated as part of the SM-D-807690-2 and -3 scanners. The discussion below derives the phase shift lens focal length. This advance is used to compensate for the phase lag introduced by detector and electronics time delay. Such delay would not interfere with a monodirectional scan system, but does interfere with a bi-directional system. In a monodirectional scanner, phase lag would cause the entire image to be translated a small amount and would not be objectionable. In a bidirectional scanner, alternate fields are scanned in opposite directions. Here even a small phase shift can be objectionable because alternate portions of lines and edges, for example, are shifted in opposite directions thus introducing distortion. Figure 3.2-16 shows an intensity profile from an edge scan with such a system, and the result achieved with a phase shift lens. The phase shift lens introduces slight positive power in the visual

rays emerging from the collimator. Motion of the scanner outer axis translates the integral phase shift lens in a direction normal to the mirror scan axis. This translation results in an apparent image displacement that leads the normal scan mirror image position by an amount dependent on lens power. Action of the optics upon translation by the scanner gimbal can thus compensate for electronic phase lag. The amount of correction required, however, is not great; for example, in a typical system operating at 30 frames per second, the detector dwell time is nominally 40 μs but the electronic time lag is only 3.6 μs (paragraph 3.4).

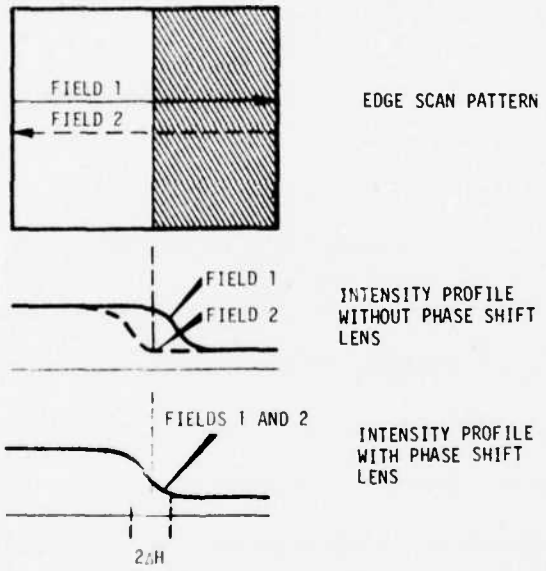


Figure 3.2-16. Electronic Phase Lag With and Without Phase Shift Lens

An equation was derived for calculating the focal length of the phase shift lens. The velocity of the image at the detector plane resulting from the horizontal scan motion is given by:

$$\dot{H} = \Delta H/\tau \qquad (3.2\text{-}7)$$

where

ΔH = image shift at detector plane

τ = electronic time constant for 50 percent step response.

This can be rewritten as:

$$\Delta H = \dot{H}\tau = F_e \cdot v \cdot \tau \qquad (3.2\text{-}8)$$

where

F_e = focal length of IR optics

v = image scan rate in object space (rad/s)

but

$$F_e = \frac{d_h}{\Delta X} \qquad (3.2\text{-}9)$$

and

$$v = \frac{2 \cdot F_r \cdot FOV_H \cdot \pi}{180 \cdot \varepsilon} \qquad (3.2\text{-}10)$$

resulting in

$$\Delta H = \frac{2 \cdot d_h \cdot \tau \cdot F_r \cdot FOV_H}{57.3 \cdot \varepsilon \cdot \Delta X} \text{ (inches)} \qquad (3.2\text{-}11)$$

where

d_h = detector horizontal dimension (in)

ΔX = detector horizontal angular subtense (rad)

F_r = frame rate (Hz)

FOV_H = total horizontal field (deg)

ε = scan efficiency.

The phase shift lens focal length, F_{ph}, can be related to the focal length of the visual collimator, F_{coll}; the phase shift requirement, $2\Delta H$ (Figure 3.2-16); and the phase shift lens translation, $\Delta\theta$: J by the similar triangle relationship shown in Figure 3.2-17. The $2\Delta H$ value can be transferred to the visual path because the IR imager and visual collimator have identical focal lengths. The image translation at the focal

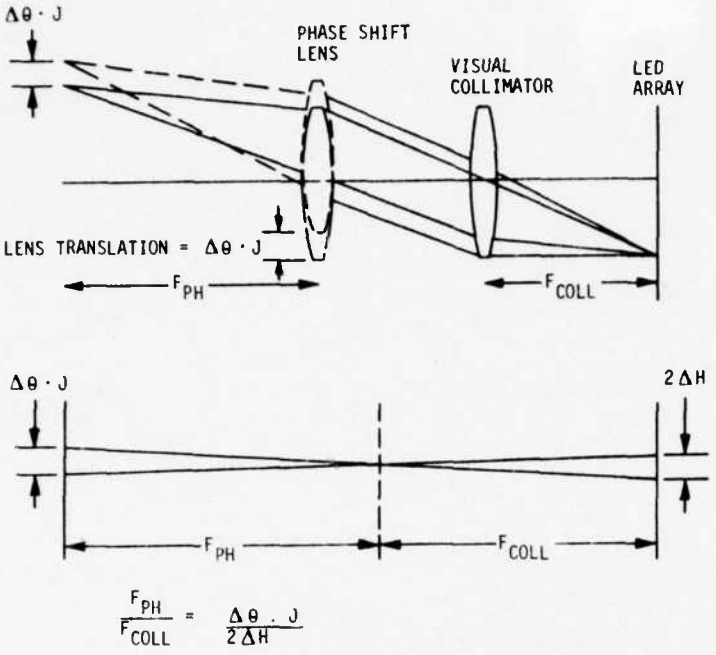


Figure 3.2-17. Phase Shift Lens Translation Geometry

plane of the phase shift lens is just the displacement of the phase shift lens because it is translating in a collimated beam. From the similar triangles, it follows that:

$$\frac{F_{ph}}{F_{coll}} = \frac{\Delta\theta \cdot J}{2 \cdot \Delta H} \qquad (3.2\text{-}12)$$

where

$\Delta\theta$ = angular rotation of the interlace gimbal, equation (3.2-1)

J = distance from phase shift lens nodal point to mechanical scanner interlace axis (1.1 inches).

Substituting for ΔH:

$$F_{ph} = \frac{(1.3)(57.3) \cdot \Delta\theta \cdot F_{coll} \cdot \Delta X \cdot \varepsilon}{(2)\ (2) \cdot d_h \cdot \tau \cdot F_r \cdot FOV_H} \quad . \qquad (3.2\text{-}13)$$

Using the collimator focal length of 2.666 inches yields the final expression:

$$F_{ph} = \frac{(42)\ \Delta\theta \cdot \Delta X \cdot \varepsilon}{\tau \cdot d_h \cdot F_r \cdot FOV_H} \quad \text{(inches)}. \qquad (3.2\text{-}14)$$

Typical values for the focal length of the phase shift lens ranges from 10 to 12 inches. The phase shift lens focal length need not be tightly controlled. Normally, a variation from the desired focal length to the actual may approach ±10 percent with no impact on system performance.

3.2.2.3 Display

There are three basic options for display of the FLIR image:

1. A monocular eyepiece can be configured for direct viewing of the LED output.
2. An image intensifier tube can be viewed directly through a biocular eyepiece.
3. A vidicon and a focusing objective lens can view the LED output for conversion to standard TV output.

This section discusses visual channel system considerations for the intensifier/biocular eyepiece display, in reference to the example system shown in Figure 3.2.-1. A monocular design may be implemented from similar considerations. Implementation of a vidicon was discussed in paragraph 3.1.3.2.3.

The major assembly of the biocular system, not discussed previously, is the visual coupling optics shown in Figure 3.2-18. The visual coupling optics focus collimated LED energy from the visual collimator common module on the image intensifier. It thus contains the phase shift lens mounted in the scanner module.

The design form is a four-element telephoto lens that achieves a 5.588-inch focal length within an overall length of 4.413 inches from the vertex of the phase shift lens to the image plane. The optical glass is the same as that used in the visual collimator common module. The design gives an

f-number of 5.0 and forms an image with a diagonal format of 40 mm to match the image intensifier (Figure 3.2-1).

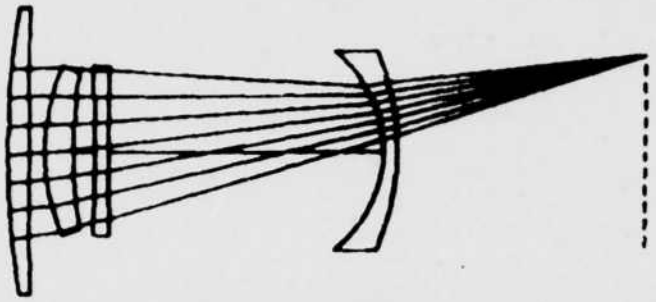


Figure 3.2-18. Optical Design Visual Coupling Optics

The power of the phase shift lens is constrained to 0.086 $inch^{-1}$ to provide the required compensation of electronic phase shift. Phase shift lens power is calculated using system parameters shown in paragraph 3.2.2.2. Significantly, the focal length of the visual coupling optics is not required to determine the power of the phase shift lens. Any visual coupling optics focal length may be used to change system magnification without changing the phase shift lens.

For the example system, Table 3.2-V lists the MTF of the visual collimator and coupling optics for the focus field points defining the half-field section of the format. A modulation of 90 percent is maintained over the half-field sectio . Modulation transfer function was calculated for up to 9.5 lp/mm, the system critical frequency at the display. Rays generating the MTF were traced at 0.645, 0.66, and 0.675 μm to match the LED output spectrum with the outside wavelengths weighted by 0.3.

TABLE 3.2-V

Visual Coupling Optics MTF

Spatial Frequency (lp/mm)	Diffraction (percent) Axial	Full-Field Vertical	Half-Field Horizontal
Scan Direction			
0.95	98	98	98
1.9	96	97	97
2.8	94	95	96
3.8	92	94	94
4.7	90	92	93
5.7	88	90	92
6.6	85	88	90
7.6	82	85	87
8.5	77	82	85
9.5	74	79	82
Vertical Direction			
0.95	98	97	98
1.9	96	93	96
2.8	94	90	94
3.8	92	87	92
4.7	90	83	90
5.7	88	80	88
6.6	85	77	86
7.6	82	73	82
8.5	77	69	78
9.5	74	65	75

Display brightness can be computed for the visual channel characteristics summarized in Table 3.2-VI. From equations (3.1.3-16) and (3.1.3-17), the display brightness is given by the relation:

$$B(fL) \frac{36 \cdot P \cdot T_{\ell} \cdot \varepsilon \cdot R_r \cdot G}{F_w^{\#2} \cdot n \cdot L^2 \cdot a \cdot R_{\ell}} \quad . \qquad (3.2\text{-}15)$$

The resultant brightness is 40 fL.

TABLE 3.2-VI

Visual Channel Characteristics

Characteristics	Symbol	Value
Image Intensifier Tube		
Luminous response	R_{ℓ}	175 μA/lm
Radiant response at 0.66 μm	R_r	0.059 A/W
Luminous gain	G	100 fL/fc
Format		40 mm (diagonal)
Output spectrum		P-20 (phosphor)
Example Display Channel		
Scan efficiency	ε	0.75
Maximum LED power (low power specification)	P	5.7 mW
Active channels	n	80
LED center-to-center spacing	L	0.004 in
Aspect ratio FOV	a	2:1
Visual relay f/number	$F_w^{\#}$	5.0
Transmission (percent)	T_{ℓ}	0.59
Visual relay		0.88
Scan mirror		0.95
Visible collimator module		0.85
Biocular assembly		0.86

3.2.3 Alignment and Setup Considerations

3.2.3.1 System Optical Alignment

The example FLIR system configuration in Figure 3.2-1 illustrates typically encountered optical train interfacing surfaces. This optical train consists of eight separate optical modules and system-peculiar assem-

blies which must interface. (The mechanical scanner and phase shift lens are considered as one.) Alignment difficulties with these assemblies are eased wherever the assemblies interface with collimated light. This is especially true of the mechanical scanner, which interfaces with the afocal assembly, IR imager, visual collimator, and relay optical assemblies. Spacing between these assemblies can be fairly flexible.

Interfaces between the remaining assemblies require more attention. The detector/dewar module requires precise axial control to position the detector array within the IR imager focus. Orthogonality requirements for lateral focus across the detector array can be largely met by provision for adjustments at the IR imager mount. At the designer's option, the imager mount can be equipped to provide spacing and tilt adjustments so that the scanner and detector/dewar modules remain fixed.

The visual collimator and LED array optical interface is established by the module design. Axial adjustment in this train can be incorporated into the coupling optics or eyepiece. Where the coupling optics are folded, it might prove practical to make this element within the assembly adjustable. Axial adjustments can be obtained by shimming, screw threads, adjustable steps, etc. The design should aim at establishing the alignments so that subsequent reassembly requires no further alignment setup, provided the same modules and subassemblies are used. The degree of adjustment required is peculiar to the system configuration and is derived from system and optical analyses and a detailed knowledge of the modules themselves. It is recommended that wherever possible the need for system-level adjustments be eliminated in favor of machined interface control. A multiplicity of adjustments, unless the design is thoroughly developed to avoid conflict between various individual requirements, can be a hindrance.

3.2.3.2 IR Imager Focal Plane Tolerance

The focal plane tolerance of the IR imager module was improved with a redesign replacing prime source TI-1173 optical material with polycrystalline ZnSe. Figure 3.2-19 shows a through-focus MTF for both the original and redesigned configurations. Details of the redesigned configuration are provided in Appendix A.10. The redesign achieved 0.0021-inch focal plane tolerance, while the original design allowed only 0.0016 inch for an increase of 30 percent. This increased tolerance improves reliability of any system using this imager.

3.2.3.3 Visual Collimator Focal Plane Tolerance

The modulation transfer of the visual collimator common module meets the requirements over a focal plane shift of 0.001 inch. This focal plane tolerance requires critical alignment of the LED array module. Figure 3.2-20 shows the relative performance of the module at 20 lp/mm in both tangential and radial orientation. A significantly larger focal plane tolerance (0.002 inch) results if only radial response is considered. Due to the aspect ratio of the elements of the LED array, the corresponding effects of degraded tangential performance of the collimator are not measurable at the system level.

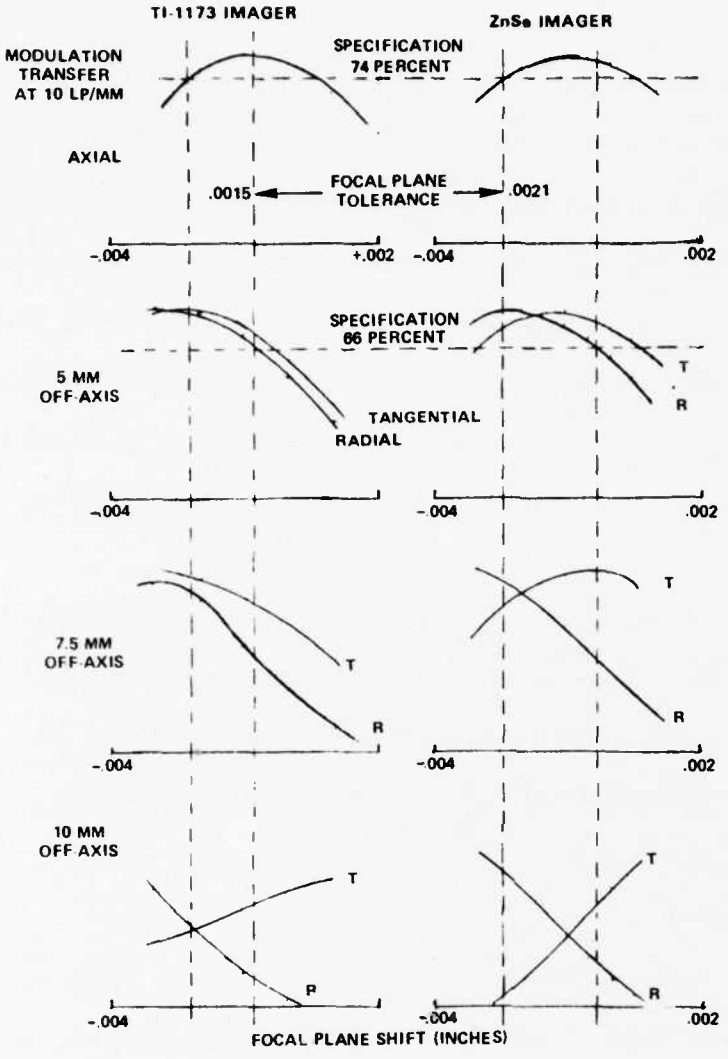


Figure 3.2-19. IR Imager Focal Plane Tolerance Comparison

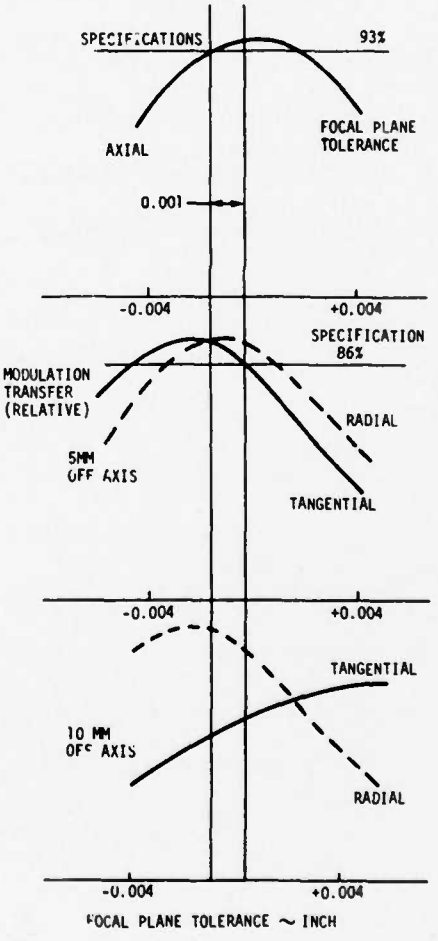


Figure 3.2-20. Visual Collimator Focal Plane Tolerance

3.3 Mechanical Design

This subsection describes module constraints, mechanical layout, recommendations, and alignment and setup procedure. Module constraints are discussed in the context of the limits they impose on the mechanical configuration for a FLIR system. Mechanical layout recommendations are provided in discussions of shape factor, mounting, access, vibration, and thermal effects. Alignment and setup procedure discussions include optical assembly interface control, mechanical scanner setup, mechanical scanner and phase shift lens balance, and cooler and detector/dewar assembly and diagnosis.

3.3.1 Module Constraints

As a first step in developing a mechanical configuration for a FLIR system, the system constraints imposed by the common modules themselves must be fully understood. The following subsection explains these constraints. Detailed characteristics of the various modules are provided in Appendix A.

3.3.1.1 Mechanical Scanner

All surfaces of the scanner housing have hole patterns for mounting. Surfaces 1, 2, and 3 are designated by the B2 specification as system mounting interfaces with a recommendation that two orthogonal surfaces be used (Figure 3.3-1). Experience has shown that the mechanical scanner is very susceptible to interlace problems if the mounting configuration follows only that guideline. Satisfactory results have been obtained by totally restraining relative motion between surfaces 1 and 3 normal, in both X and Y directions, to the scan axis. A variety of approaches are open to the designer in interpreting

this into the structural support. No single option can meet the diverse requirements imposed by different system applications. The designer should bear in mind that motion along the scan axis has little effect on scanner performance. This allows the support structure to easily accomodate any height tolerance when scanners are interchanged in a FLIR system. It will probably be necessary to adjust the scanner interlace after the scanner is mounted because the interlace can be affected by the mounting.

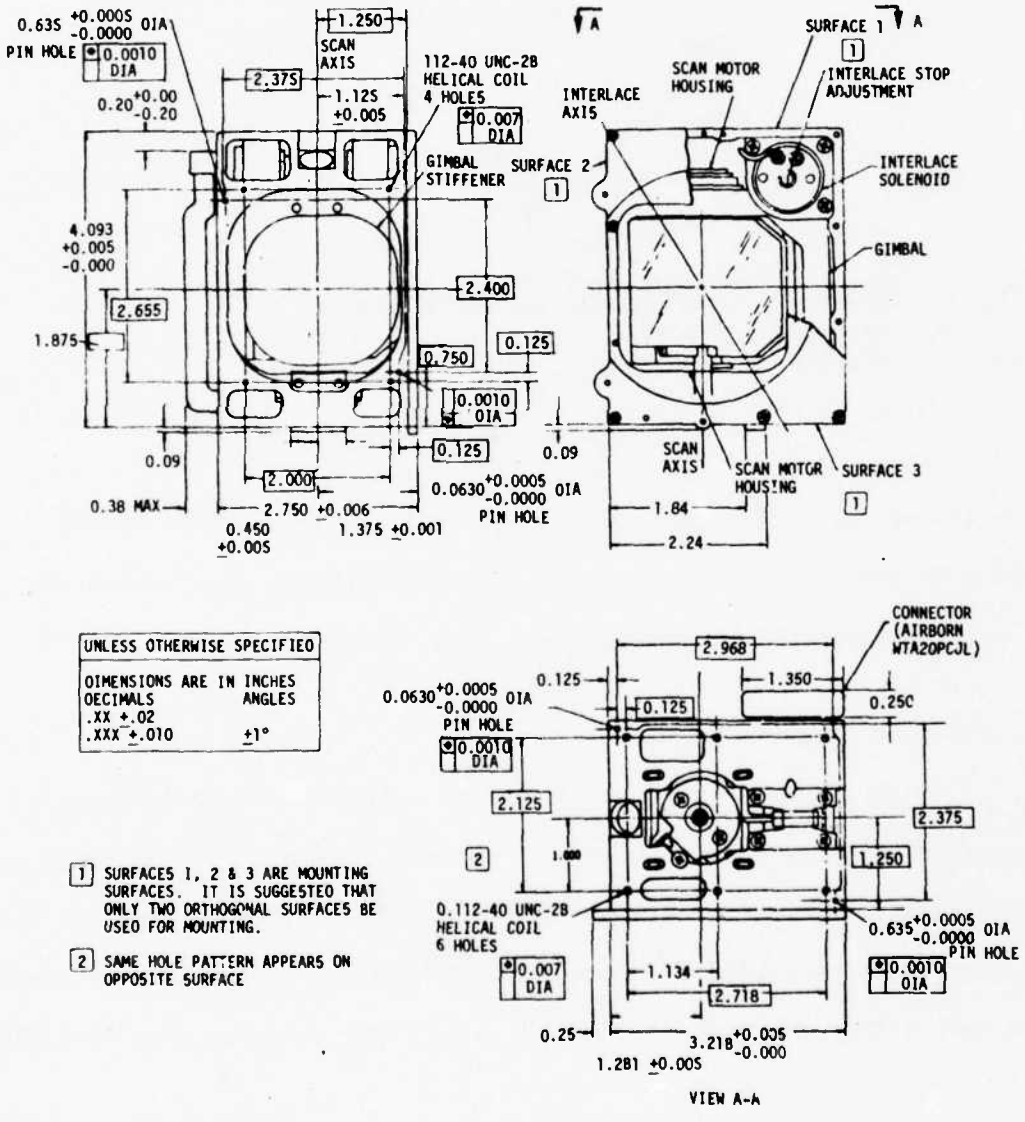
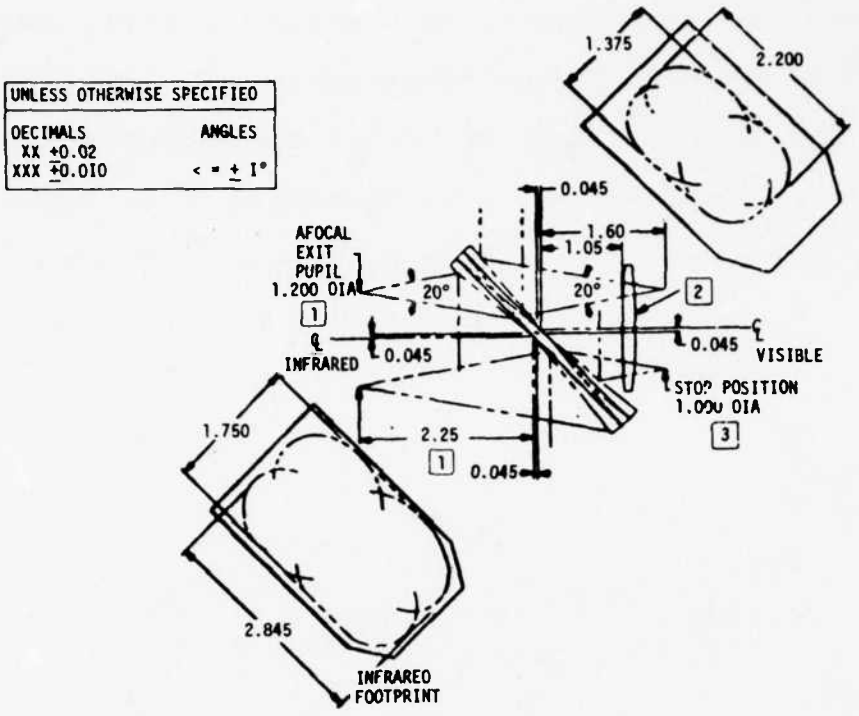


Figure 3.3-1. Scanner Outline Dimensions



1. THESE DIMENSIONS VARY FOR DIFFERENT AFOCAL DESIGNS.
   EXAMPLE: IF 1.200 DIM. IS SMALLER, THEN 2.25 DIM. CAN INCREASE
2. PHASE SHIFT LENS IS OPTIONAL.
3. MAY VARY IN LOCATION IF SMALLER.

Figure 3.3-1. (Cont)

The scanner electrical interface is provided by a 20-pin connector (SM-C-773254-1) pigtailed from the scanner assembly. The system mating connector is similar to the Airborn, Inc., connector WTA20SECJTA.

3.3.1.2 IR Imager

The IR imager (Figure 3.3-2) module is provided with an interface for mounting directly to the mechanical scanner. However, depending on system ray traces, it could be spaced out from the housing and a separate mounting structure provided. This spacing flexibility can be used to advantage in controlling the system envelope. A gear-cut focusing ring is built into

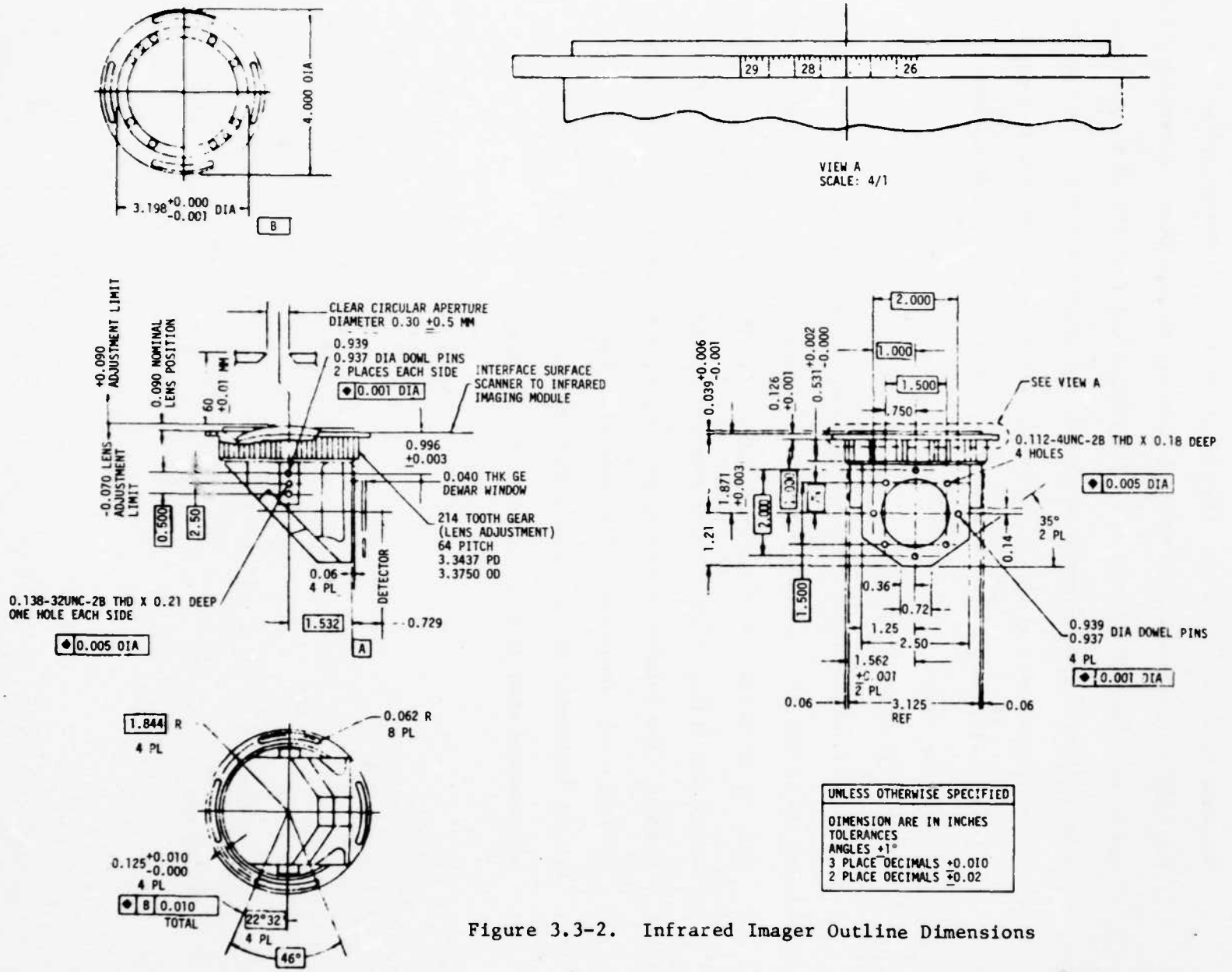


Figure 3.3-2. Infrared Imager Outline Dimensions

the imager, and system use of this would athermalize the IR optical chain. The mode of operation of this fine-focus control is a design option, and the module incorporates two mounting pads for this purpose. Athermalization can be achieved for the system by including a drive to the IR imager focus ring, either operator-command or closed-loop automatic servo. The surface at the exit element of the IR imager is provided with a bolt-hole pattern and dowel alignment pins. This is available for optional system devices between the imager and detector window.

3.3.1.3 Visual Collimator

The interface for the visual collimator (Figure 3.3-3) can be direct to the mechanical scanner; however, care must be exercised to retain clearance to the moving parts of the scanner. As with the IR imager, system optics ray traces allow some designer options in actual spacing from the scanner. The collimator interfaces directly with the LED array for correct spacing to the field-flattening element in the LED array module. The visual collimator is rear-mounted when mounted opposite the afocal and side-mounted when directly opposite the IR imager.

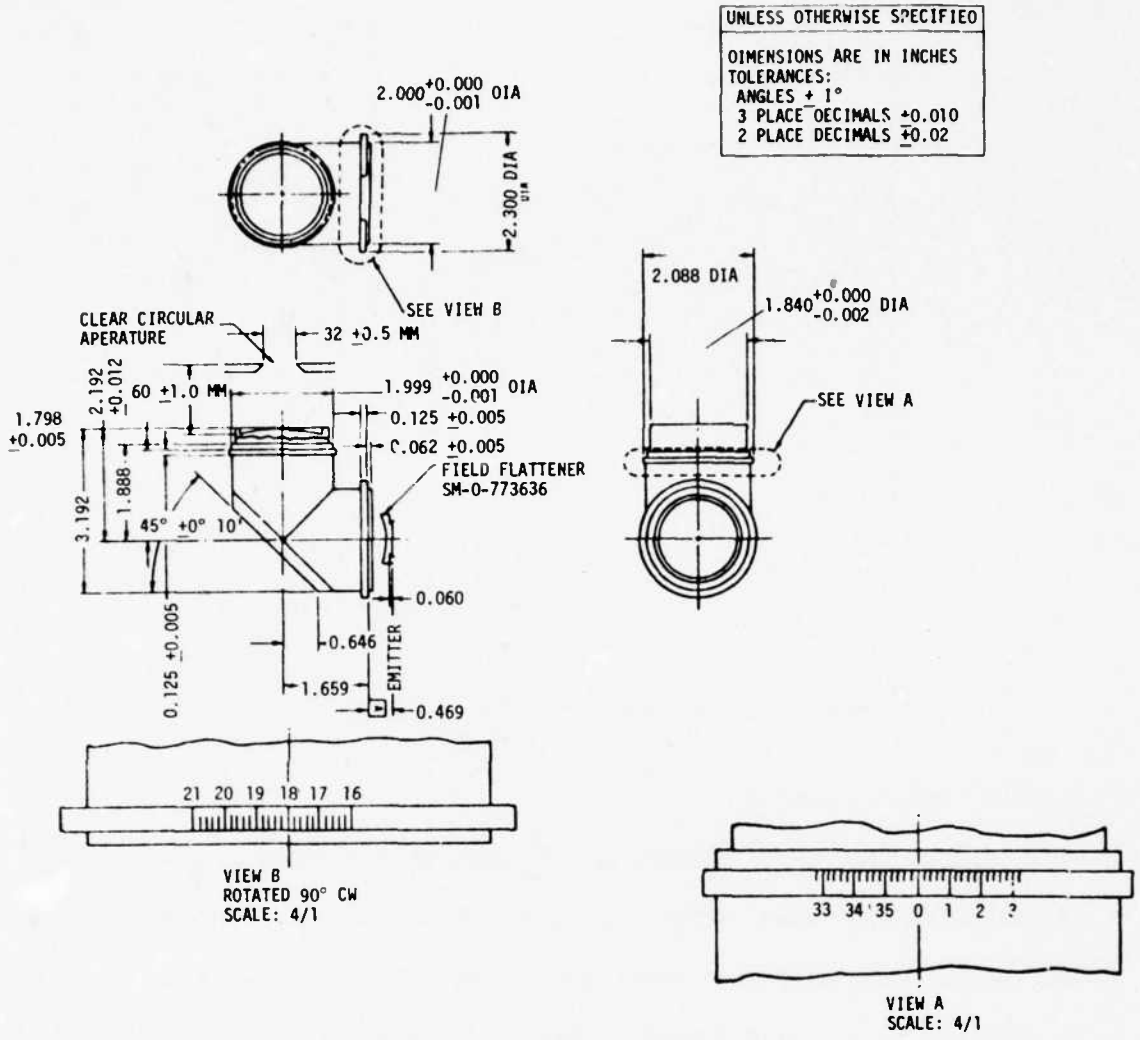


Figure 3.3-3. Visual Collimator Outline Dimensions

3.3.1.4 LED Array

The LED array (Figure 3.3-4) has flanges that interface with those of the visual collimator. A clamping action between them is a design option. Also, the LED array has four captive screws for its own system interface. The LED electrical interface is provided by a two-section connector (SM-D-773627), each section containing 114 pins. The system mating connector (one for each section) is similar to SM-C-772563-1.

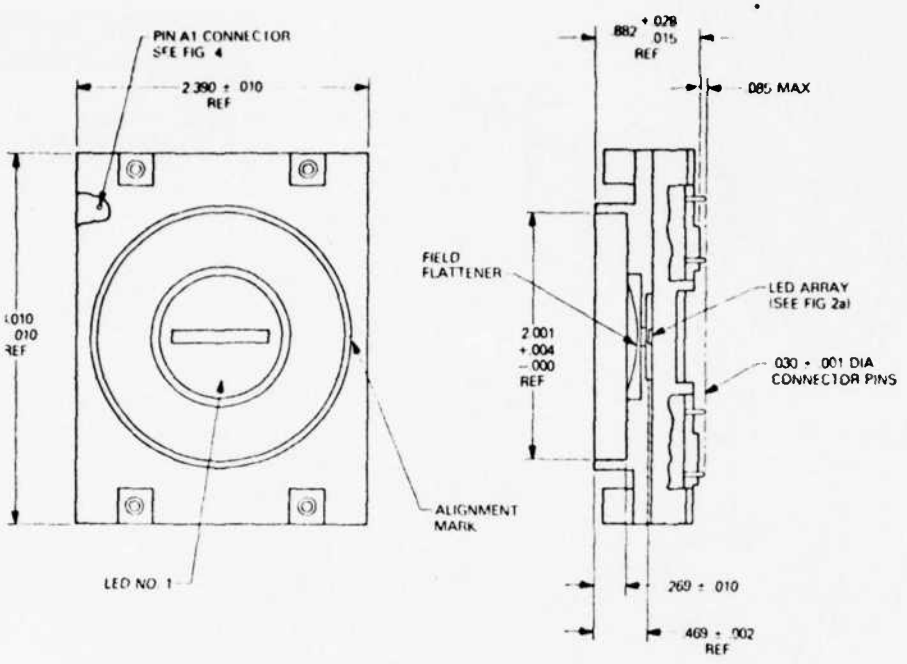


Figure 3.3-4. LED Array Outline Dimensions

3.3.1.5 Detector/Dewar

The detector/dewar (Figure 3.3-5) must be precisely located on the IR imager optical axis. The rear flange incorporates a system-interface bolt pattern and alignment dowel pins. The detector electrical interface is provided by a four-quadrant receptacle. Each quadrant is a 59-pin connector (SM-C-773261-1). The system mating connector (one for each quadrant used) is similar to the Airborn, Inc., connector WTA59SFJT594. Figure 3.3-6 shows connector details.

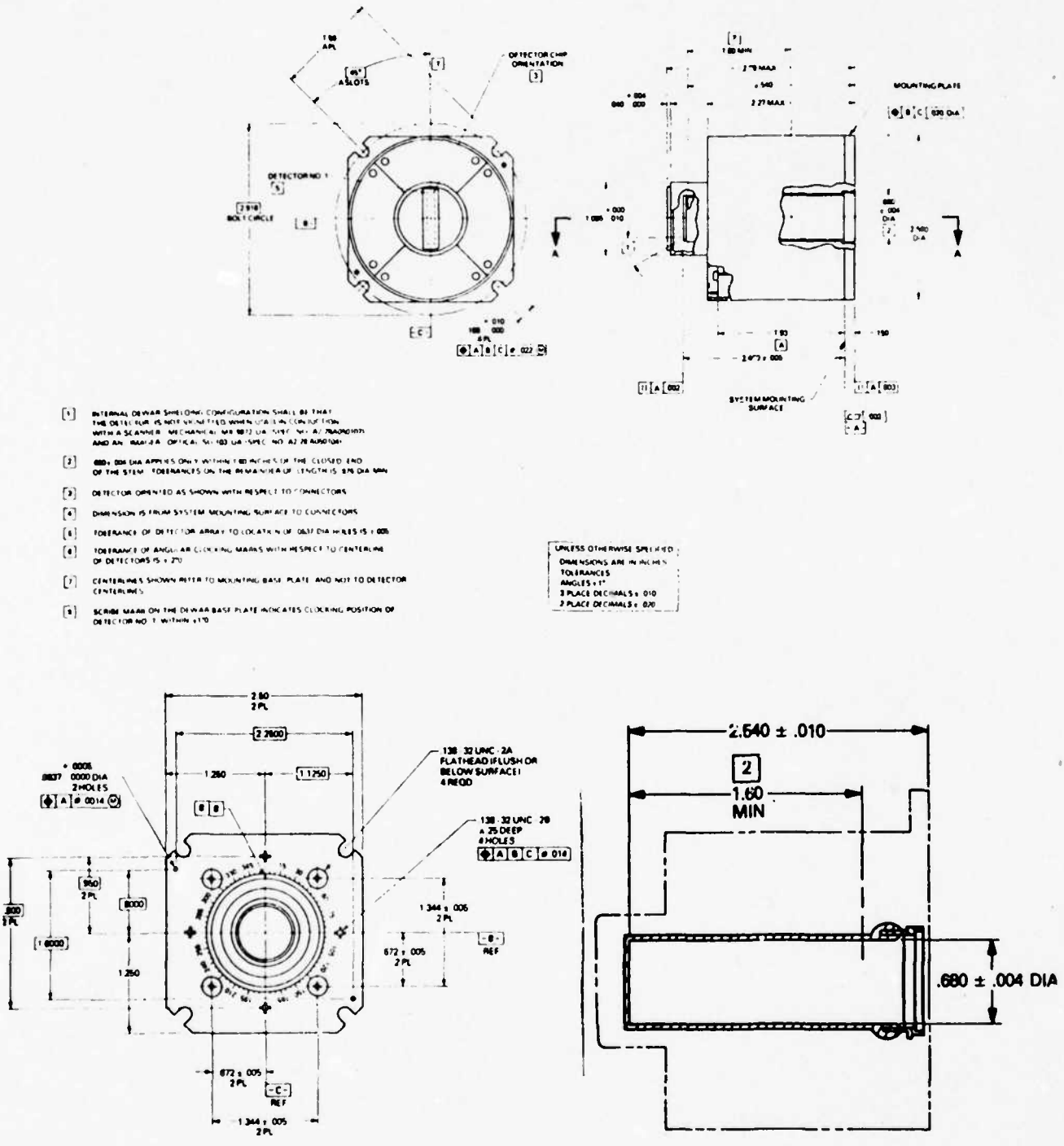


Figure 3.3-5. Detector/Dewar Outline Dimensions

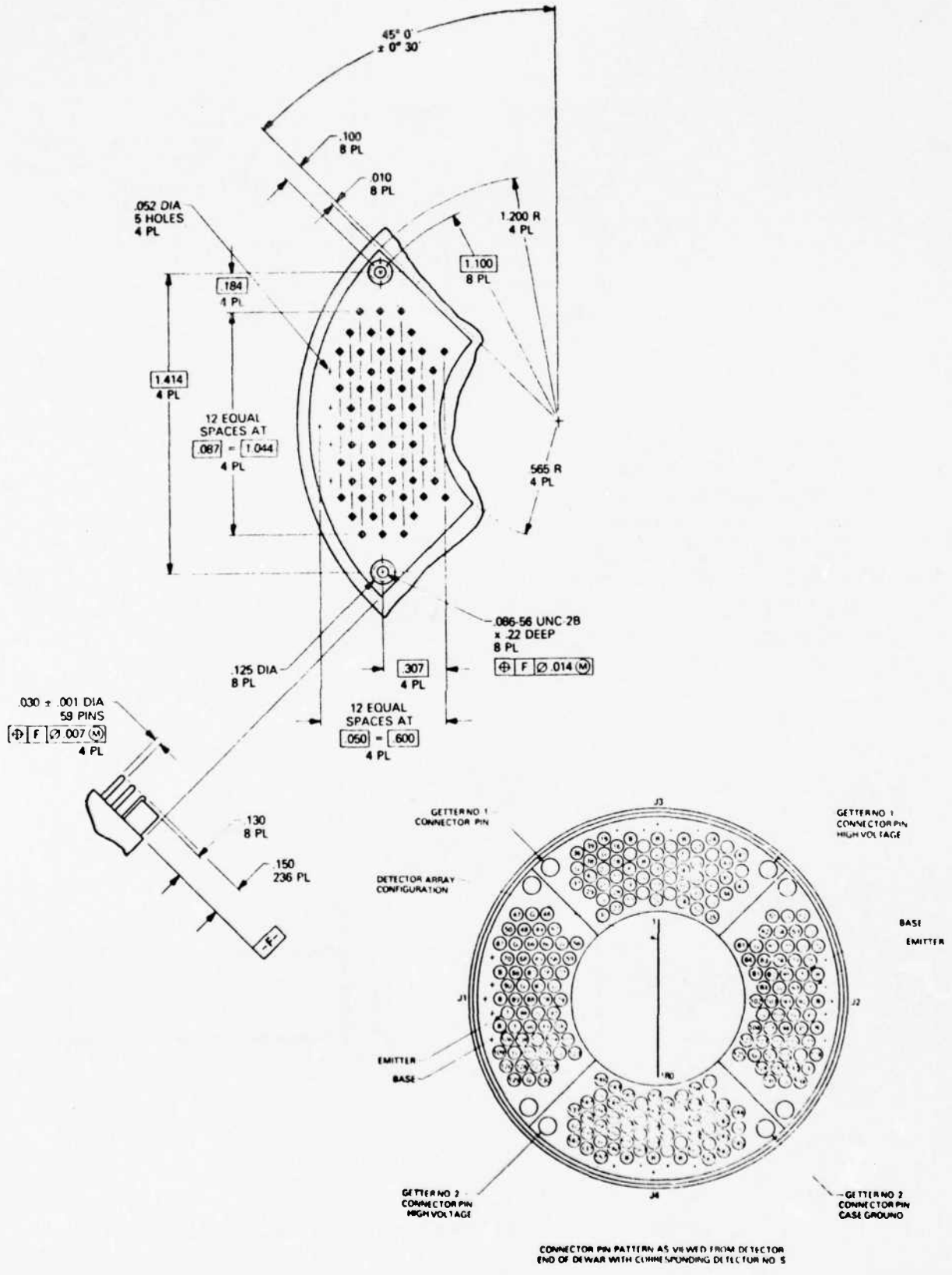


Figure 3.3-6. Detector/Dewar Connector Details

The module is also provided with an interface for subassembly with the cooler common module. This is a symmetrical four-hole pattern which enables the cooler to be oriented in any of four 90-degree positions. Due to the fragile nature of the dewar and its susceptibility to damage by the cooler cold finger, these two modules should be maintained as a subassembly whenever possible. This is further stressed by the requirement for the dewar and cold finger assembly to be made in a dry nitrogen atmosphere. The detector/dewar interface flange cannot be considered adequate to also carry cooler loading.

3.3.1.6 Cooler

The cooler (Figure 3.3-7) must be mounted in a system by utilizing the threaded mounting holes in either the cylinder head or the base drive. Since the detector/dewar is mounted to the cold finger flange, the cooler mounting arrangement must provide for precise location of the flange in order to ensure correct detector/dewar location. Some flexibility in mounting is available since the cooler can be oriented relative to the detector/dewar in any of four positions* which are 90 degrees apart. This mounting flexibility can be advantageous in controlling the system envelope. Forced air circulation over the cooler housing fins must be supplied unless a large, efficient heat sink is utilized. In either case, sufficient cooling must be provided to ensure that the housing temperature does not exceed 15°C above ambient. The cooler must be provided with 117V, 400 Hz power by means of a 4-pin connector similar to a Winchester Electronics Number JF3SIPABD. The power requirement is approximately 70 watts during startup and 40 watts during normal operation.

*There is no constraint to these four positions; the relative orientation can be at any angle since the dewar base rotates independently of the array.

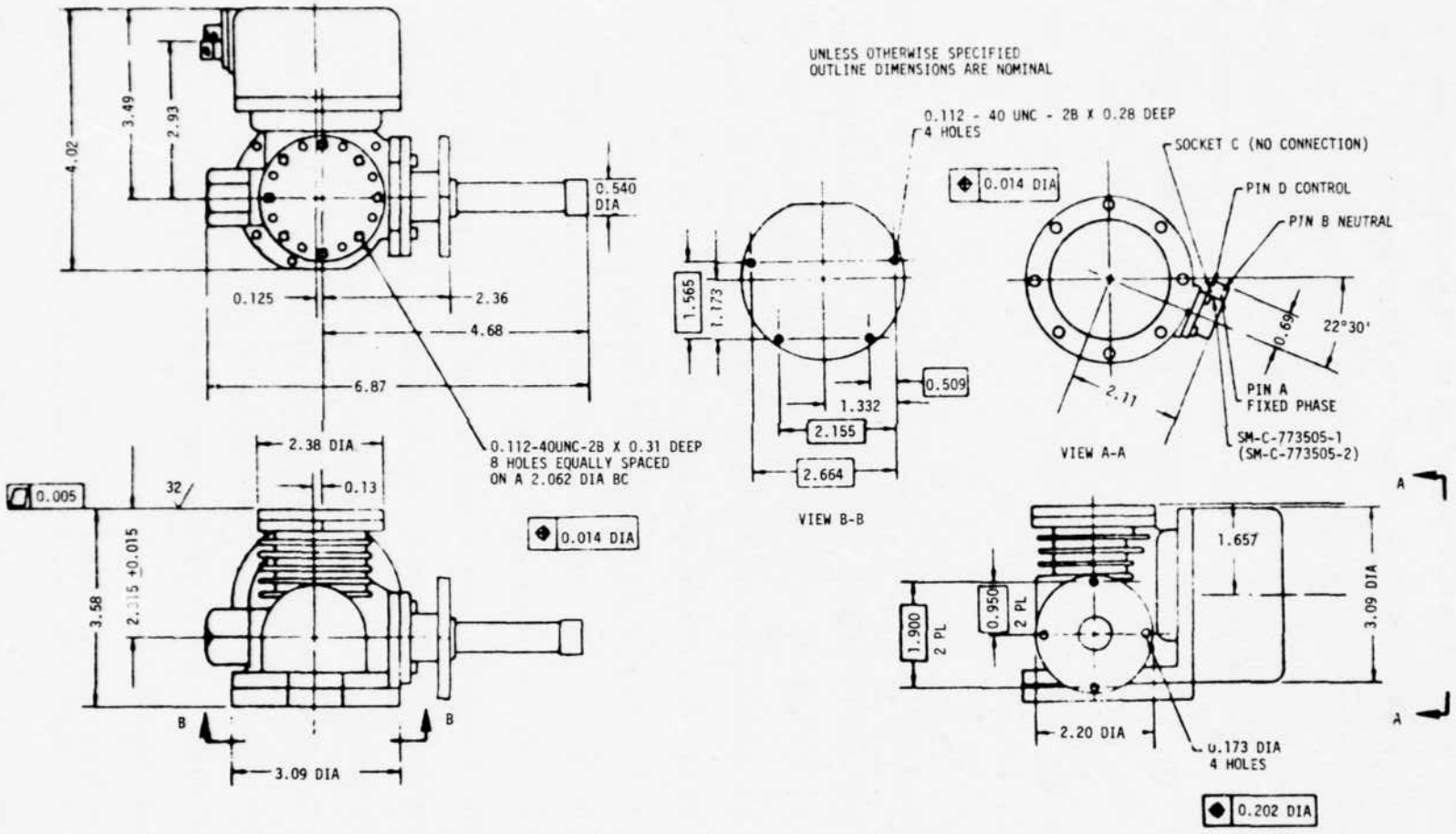


Figure 3.3-7. Cooler Outline Dimensions

3.3.1.7 Inverter

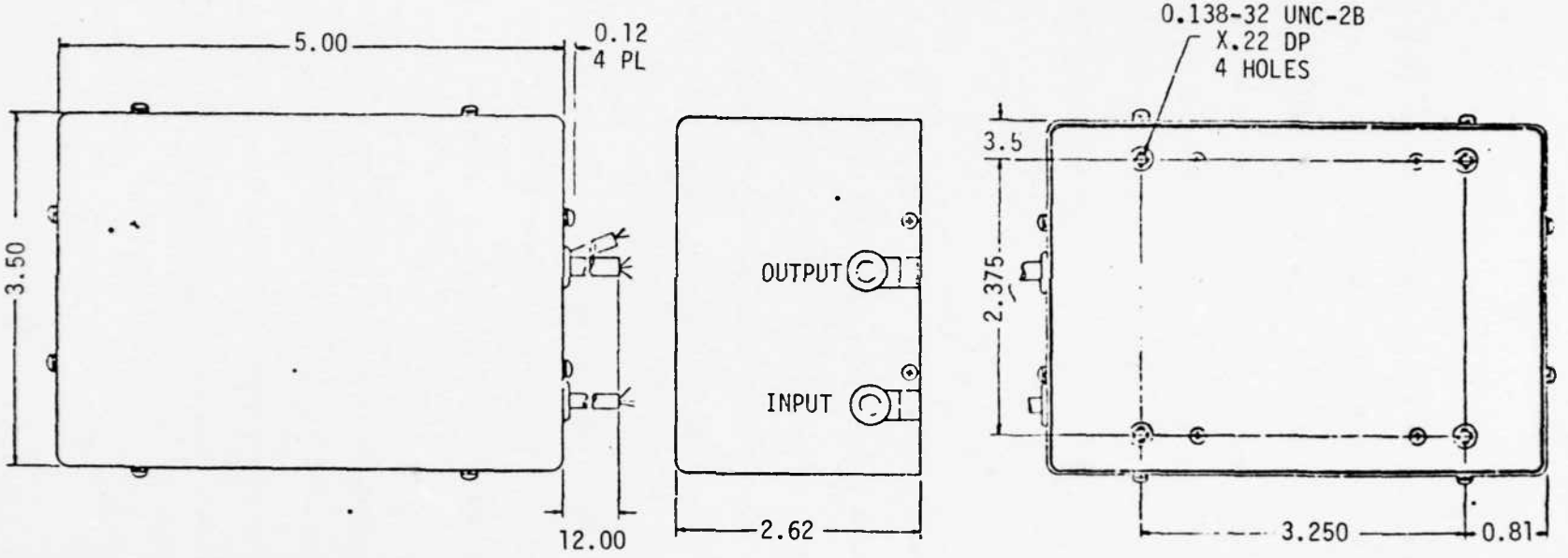
The inverter module (Figure 3.3-8) system interface is provided by a mounting hole pattern incorporated in the base plate. The dc/ac inverter electrical interface is provided by an eight-wire pigtail, which may be terminated in a connector or a terminal strip as system interconnection requires. System usage of the inverter can be considered an option when only 24 Vdc is available to power the modular cooler. Although the inverter is an electronic common module, it is treated spearately here because of its size and interface requirements.

3.3.1.8 Electronic Common Modules

The electronic common modules (Figures 3.3-9 through 3.3-13), preamplifier, postamplifier/control driver, bias regulator, auxiliary control, and scan and interlace, are single printed circuit boards and are designed for mounting in card guides. The preamplifier and postamplifier/control driver modules have connectors both top and bottom. The top connectors are for board-to-board connection, and the bottom connectors include the provision for interconnect to the detector/dewar in the case of the preamplifier modules, or to the LED array in the case of the postamplifier/control driver modules.

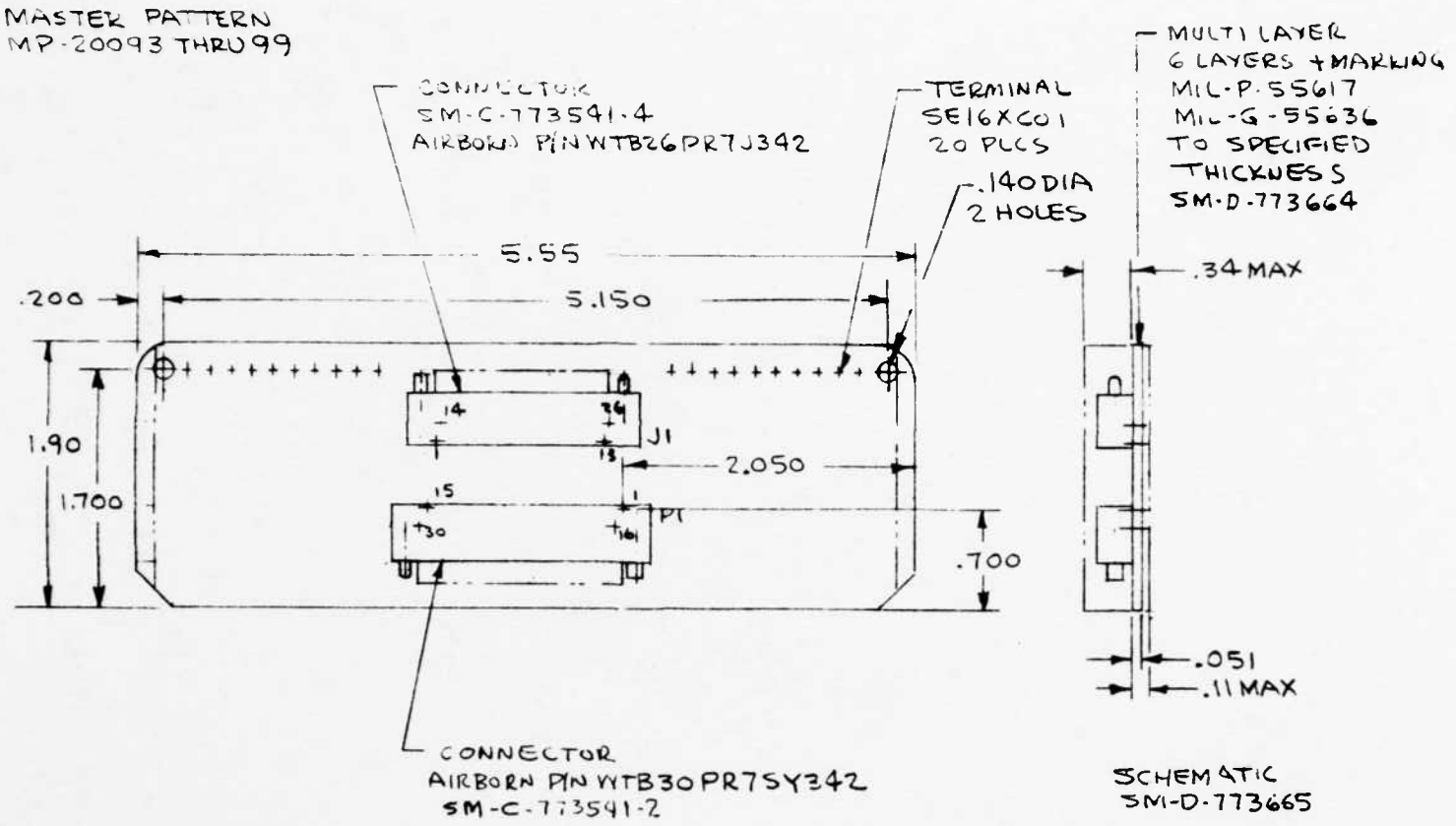
Lead length to the detector and LED array is important in controlling system noise, and the detector leads are of prime importance. Efforts must be made both in shielding exposed leads and in maintaining the amplifier stages in separate EMI-proof enclosures to obtain optimum performance of the system.

B2-28A050108
28 June 1974



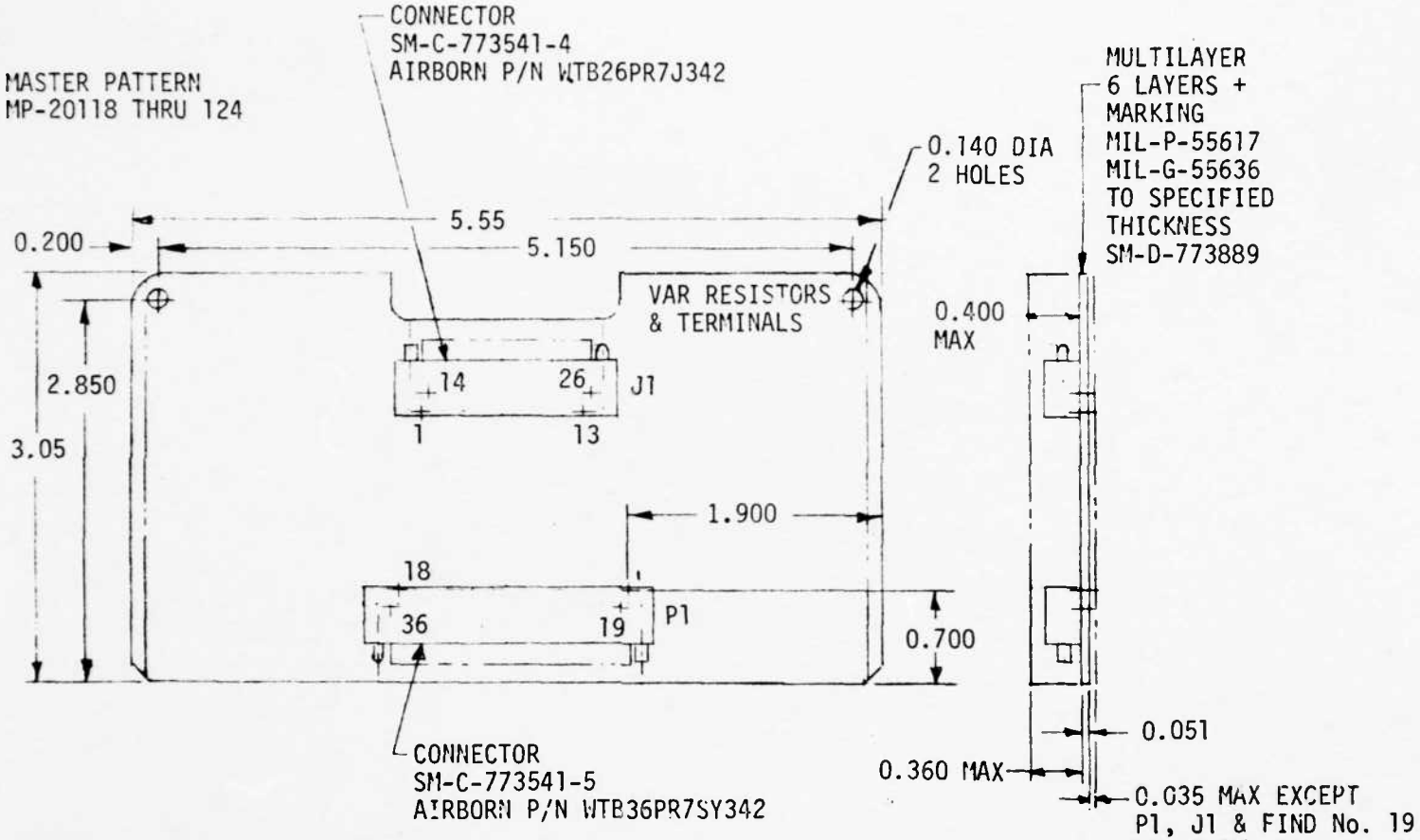
NOTE: WEIGHT 2.9 LB MAX

Figure 3.3-8. Inverter Outline Dimensions



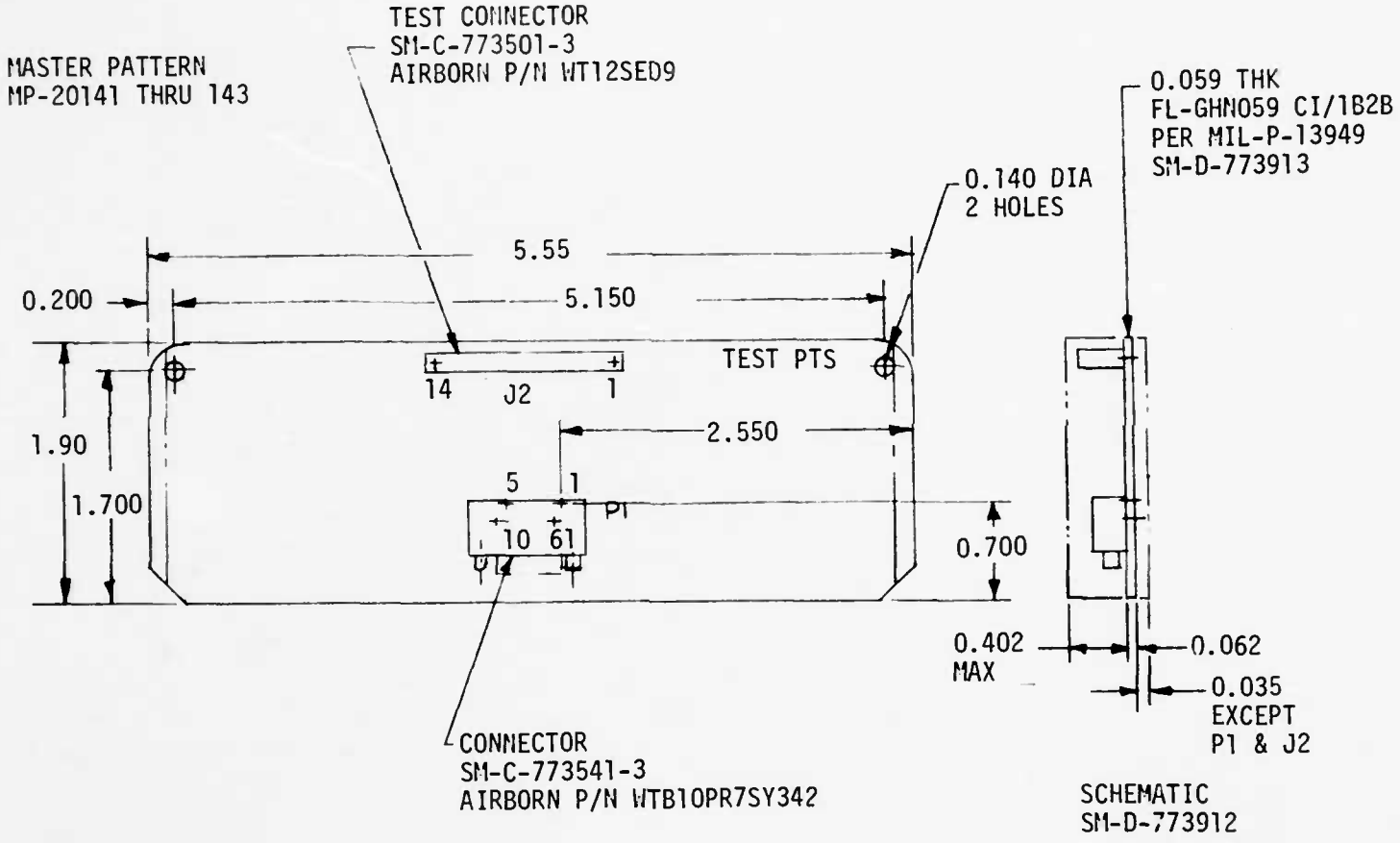
NOTES: 1. WEIGHT 0.16 LB ±10%
2. MATING CONNECTORS SIMILAR TO
36 PIN - AIRBORN WTAX36PD9SYL
26 PIN - AIRBORN WTAX26SED9STA

Figure 3.3-9. Preamplifier Outline Dimensions



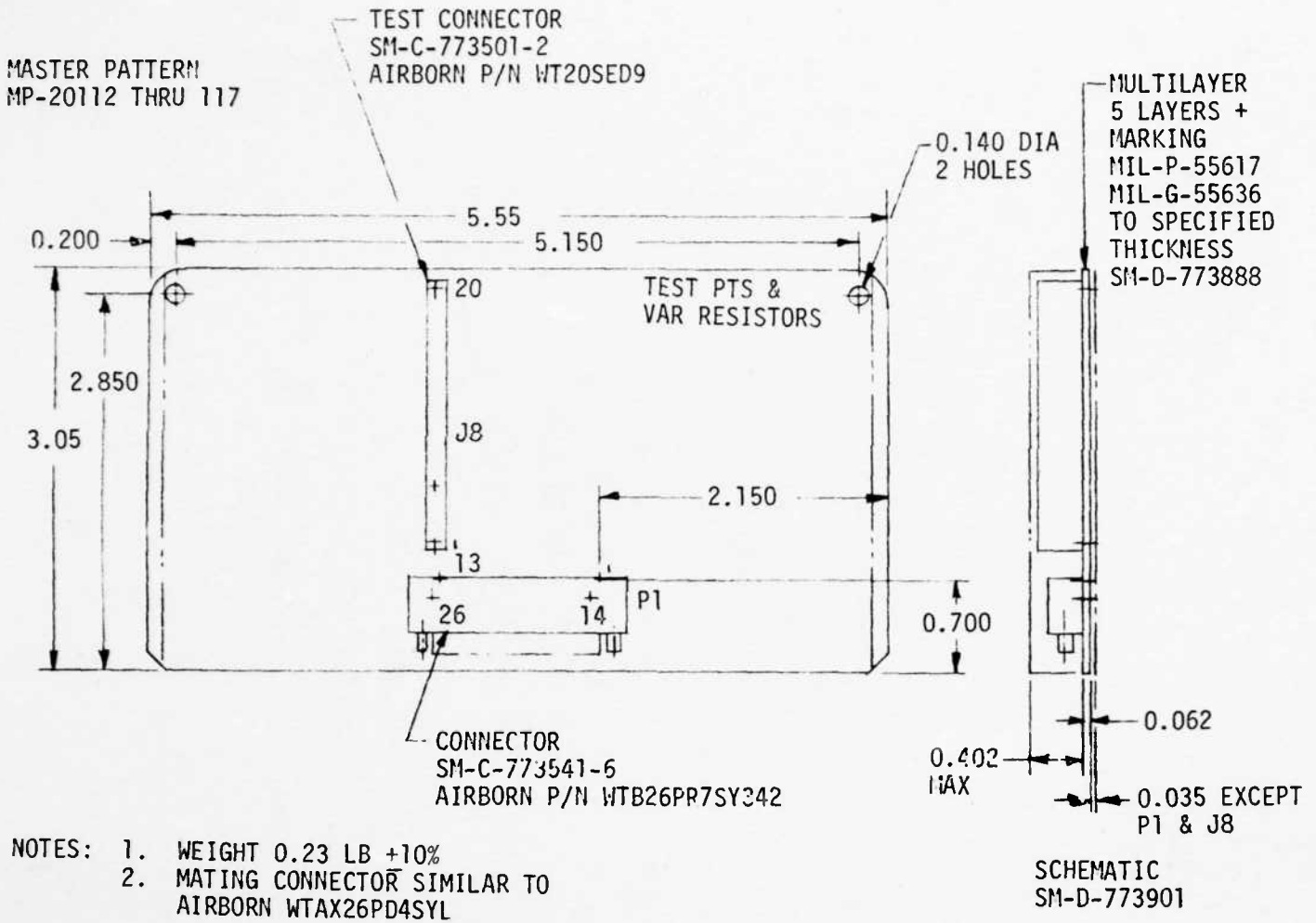
NOTES: 1. WEIGHT 0.26 LB +10%
2. MATING CONNECTORS SIMILAR TO
36 PIN - AIRBORN WTA36PD9SYL
26 PIN - AIRBORN WTA26SED9STA

Figure 3.3-10. Postamplifier/Control Driver Outline Dimensions



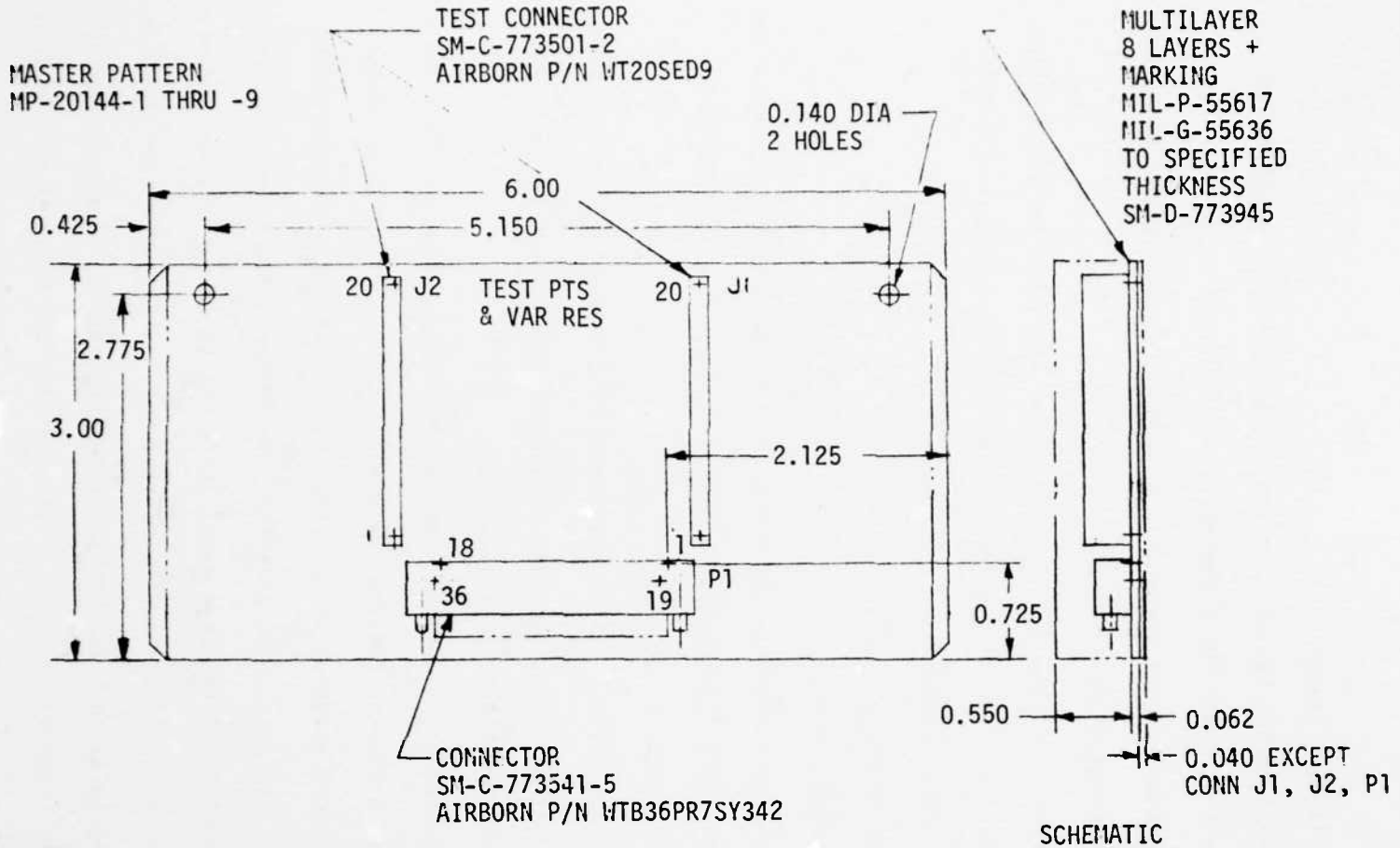
NOTES: 1. WEIGHT 0.16 LB +10%
2. MATING CONNECTOR SIMILAR TO AIRBORN WTAX10PD9SYL

Figure 3.3-11. Bias Regulator Outline Dimensions



NOTES: 1. WEIGHT 0.23 LB +10%
2. MATING CONNECTOR SIMILAR TO AIRBORN WTAX26PD4SYL

Figure 3.3-12. Auxilliary Control Outline Dimensions



NOTES: 1. WEIGHT 0.35 LB MAX
2. MATING CONNECTOR SIMILAR TO AIRBORN WTB36SECSY

Figure 3.3-13. Scan and Interlace Outline Dimensions

3.3.2 Mechanical Layout

To complete the system, certain system-peculiar assemblies are required. In a typical direct viewing system, these include:

1 Afocal entrance optics - a collimator gathering the IR energy to image on the detector

2 Visual coupling optics - the system phase shift lens mounting into the interlace gimbal, relay imaging optics, and system viewing eyepiece

3 System power supply

4 System controls.

System-peculiar assemblies and the support structure itself constitute the only design options available in system volume and weight control.

3.3.2.1 Shape Factor Control

There are certain built-in features of the modules that aid in system volume and shape factor control. These are in addition to those noted for the separate modules in paragraph 3.3.1.

The IR imager, visual collimator, detector/dewar, and LED array are equipped with angular scales. This aids in image orientation control. The recommended practice is to orient the mechanical scanner so that the scan is horizontal to the scene. The detector/dewar and LED arrays must then be parallel to the scan axis. Both the IR imager and the visual collimator include a folding mirror. Therefore, it is possible to rotate either optical module as long as the associated array is also angularly displaced to preserve image orientation. This provides the designer with a good degree of latitude in determining an optimum system shape factor for different common module applications.

3.3.2.2 Mounting

Possible system applications can vary widely. One common feature of any electro-optic system, however, is the need for a stiff and stable structural base. The mounting of all system optics to a common optical bench structure is a recommended design goal.

Because most systems are controlled by a weight budget, stiffness must be gained through the use of lightweight structure. The structural design must not allow vibrational excursion to affect optical resolution during system operation, nor can yielding of any structure be tolerated.

3.3.2.3 Access

A housing seal must be provided without adversely affecting system maintenance. The system requires a sealed, dry environment to maintain performance in a typical climate spectrum. Typically, this is achieved by pressurizing the system with dry inert gas and enabling a periodic atmospheric purge. Another method is the use of a dessicant breather system. Direct access should be available to all common module interfaces and adjustment features without the need for removal of subsystem components or other common modules.

3.3.2.4 Vibration Control

The individual modules are tested in both shock and vibration per their specification. However, exposure at the system level can include dynamic amplification by the structure. Wherever possible, the design should consider the use of isolation methods and damping structure.

3.3.2.5 Thermal Considerations

The combined module heat dissipation for a 180-channel system with the closed cycle cooler is on the order of 110 to 120 watts with approximately

50 percent of this total from the cooler. In general, the individual module specifications call for operation in a 160°F environment, and system requirements will usually specify operation at temperatures up to 125°F. Unless high packaging density is employed in the system layout, active cooling will not be required for the modules with the possible exception of the cooler. Most of the heat generated in the cooler is in the motor windings and the compression space, both of which are housed in finned aluminum castings.

The cooler should be mounted so that the compression head is heat sunk to the system structure, or so that the finned surfaces on the motor housing and compression space can be cooled by forced convection using a small blower. Sufficient cooling must be provided to ensure that the housing temperature does not exceed 15°C above ambient. Although active cooling other than this small blower will probably not be required, a system thermal analysis should be included as part of the mechanical design to ensure that operational temperatures will not be exceeded and that the mounting and packaging techniques provide for good thermal dissipation.

The specific thermal interfaces that must be considered in installing the cooler in a system are: compressor head and heat sink, cold-finger-bellows glass stem assembly, and cold finger flange and detector/dewar flange. Appendix A.9 describes the various features of the cooler module assembly. The compressor head and heat sink interface serves two functions: it structurally supports the cooler and it provides a heat conduction path to a structural sink. Thus, the compressor head should be rigidly mounted to the heat sink, using a mounting technique that will not loosen due to vibrations induced by the cooler drive assembly. The heat sink surface

that contacts the compressor head surface should be smooth and flat. A thermally conductive grease should also be used between these two surfaces to minimize thermal contact resistance.

The cold-finger-bellows glass stem assembly interface forms a portion of the thermal conduction path between the cold expansion volume and the thermal load (detector elements and vacuum dewar). Thus it is important that the thermal contact resistance at this interface be kept to a minimum. When mating the cooler to the detector/dewar, the assembly procedure discussed in paragraph 3.3.4.1 must be followed carefully to ensure minimum contact resistance and to avoid damaging the detector/dewar. When mated, the spacing between the end of the cold finger and the inner surface of the glass stem provides for approximately 0.03 inch of compression in the bellows.

The cold finger flange and detector/dewar flange interface provides an O-ring seal of the volume contained between the outside of the cold finger tube and the inside of the glass stem assembly. The cold-finger-bellows glass stem assembly interface is contained within this volume, and it is important to maintain good thermal contact at this interface. Thus the cooler and detector/dewar should be mated in an inert gas environment, and the seal at the cold finger flange and detector/dewar flange interface should ensure that the inert gas remains sealed in this volume.

3.3.2.6 Example Layout

A typical FLIR system layout is shown in Figure 3.3-14. The imaging modules are shown in the rear-mount configuration. The amplifier stages are shown in a separate EMI-shielded enclosure; the enclosure would further separate the preamplifier and postamplifier stages with a metal divider panel.

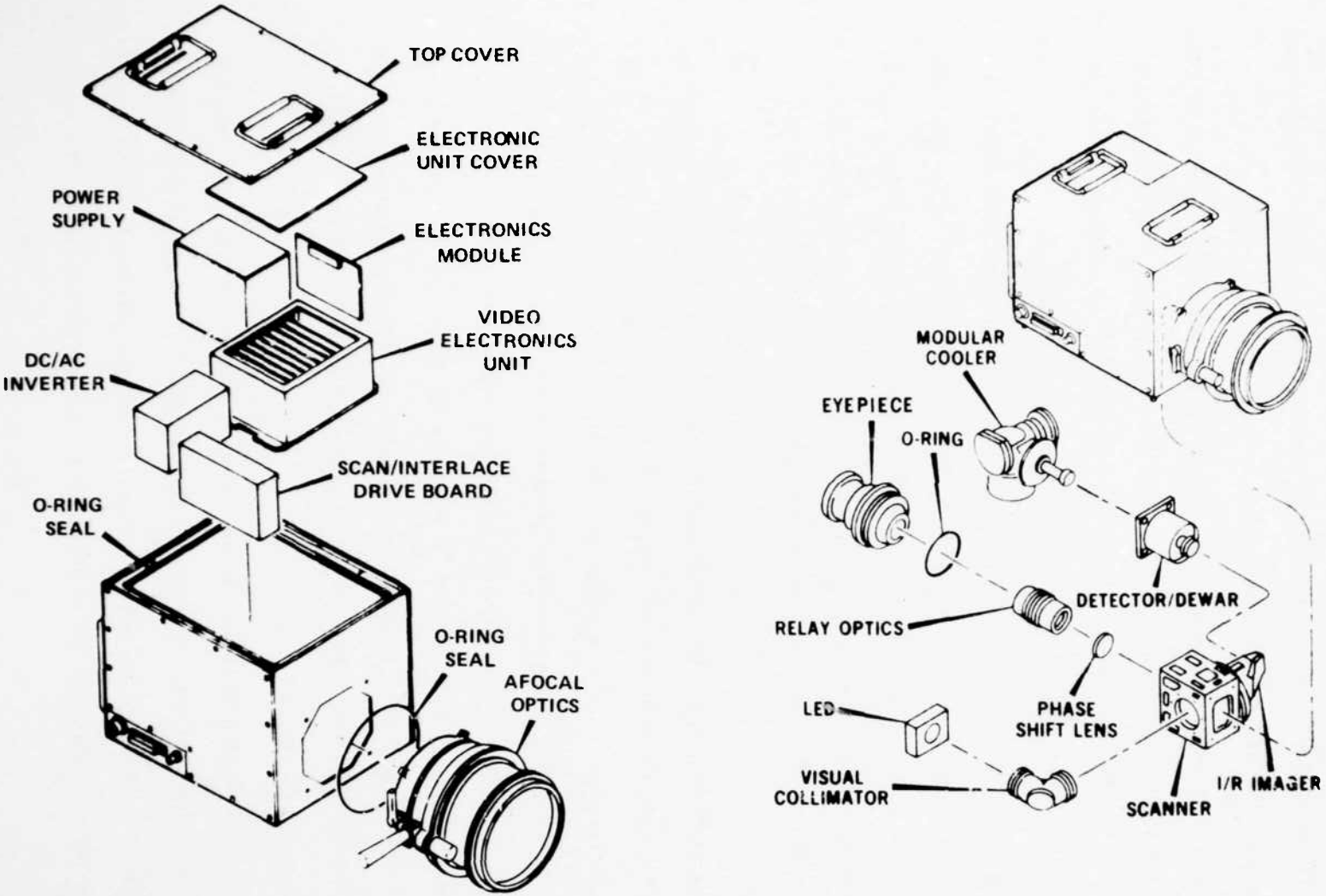


Figure 3.3-14. Typical FLIR System

3.3.3 Alignment and Setup Considerations

3.3.3.1 Interface Control

Many of the alignment and setup practices recommended in paragraph 3.2.3 apply to mechanical as well as optical design requirements. Close liaison is required between structural and optical designers. As with any folded optical system, precise interface control is required between modules to maintain optical performance. Wherever possible, the common module interface should be used directly, and the use of shims should be limited. This will aid in achieving module interchangeability.

3.3.3.2 Mechanical Scanner Setup

The mechanical scanner is described by Figure 3.3-1 where overall size and weight are shown. The scanner is supplied with a pigtail connector for system electrical interconnect to power and control circuitry. Other scanner details are shown in Figure 3.3-15.

Three functions of the scanner are driven by electronic controls: the mirror scan rate, mirror angular travel, and interlace gimbal travel.

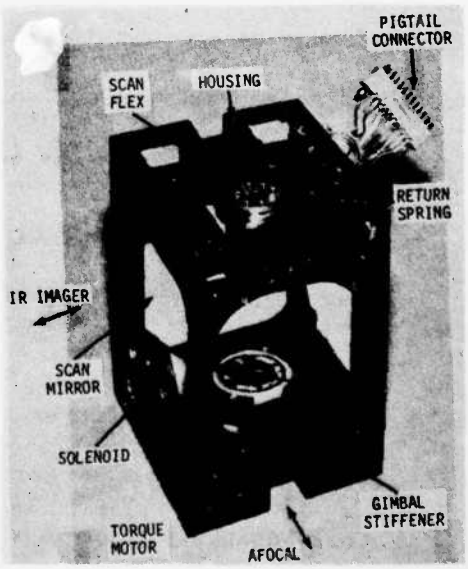


Figure 3.3-15. Mechanical Scanner

For each function there is a corresponding mechanical adjustment. For example, the scanner assembly is supplied with interchangeable mirror return springs of 30 and 60 Hz nominal ratings. Selection must be a system choice based on performance evaluation. In addition, spring mounts allow for adjustment of scan mirror angular travel. This can be calibrated by mechanical or electro-optical test methods before locking the return springs into position.

Interlace axis travel is accomplished by the two solenoids. Each solenoid plunger assembly incorporates an interlace travel stop with a screw thread adjustment. The electro-optical requirement for interlace axis excursion can be interpreted as a precise linear displacement at some radius to the axis. This displacement can then be achieved by adjusting the limit stops before locking the threads in position.

3.3.3.3 Cooler and Detector/Dewar Setup

3.3.3.3.1 Assembly Procedure

This procedure establishes a method of assembly for the cooler and detector/dewar to prevent damage to the dewar and to establish a good thermal interface between the cooler and detector/dewar. Figure 3.3-16 illustrates the cooler and the detector/dewar assembly.

Dewar installation involves the following steps:

1 Check that the bellows will slide smoothly over the cooler cold finger.

2 Coat cooler cold finger surface A with a thin coat of thermal compound such as Dow Corning Wakefield type 120 thermal compound.

3 Coat bellows surface B with a thin coat of thermal compound.

4 Install the bellows onto the cold finger.

5 Insert four screws with split washers in the small holes of the cooler cold finger flange.

6 Install the O-ring in the groove of the dewar.

NOTE: Steps 7-12 should be performed in an inert atmosphere.

7 Set the cooler (head up) and dewar on a flat surface as shown. Make certain the dewar is oriented as required by the system application.

8 Carefully slide the dewar onto the end of cooler cold finger until the bellows touches the glass stem.

9 Start the two opposite side screws and evenly snug them up to the O-ring by hand.

10 Tighten the two side screws by turning 1/4 turn in sequence until the flanges meet. Observe the gap during tightening and maintain parallelism.

11 Insert the top and bottom screws and tighten them.

12 In sequence, check all screws for tightness.

Dewar removal involves the following steps:

1 Ensure that the detector and cooler cold finger are at room temperature. If in doubt, allow 2 hours of nonoperating time before removal.

2 Remove the top and bottom screws.

3 Set the cooler and detector/dewar (head up) on a flat surface.

CAUTION: Follow steps 4 through 6 carefully because the glass stem is easily damaged.

4 Remove the side screws by turning each 1/4 turn in sequence.

5 Withdraw the dewar from the cold finger.

6 Remove the bellows from the dewar stem or cold finger.

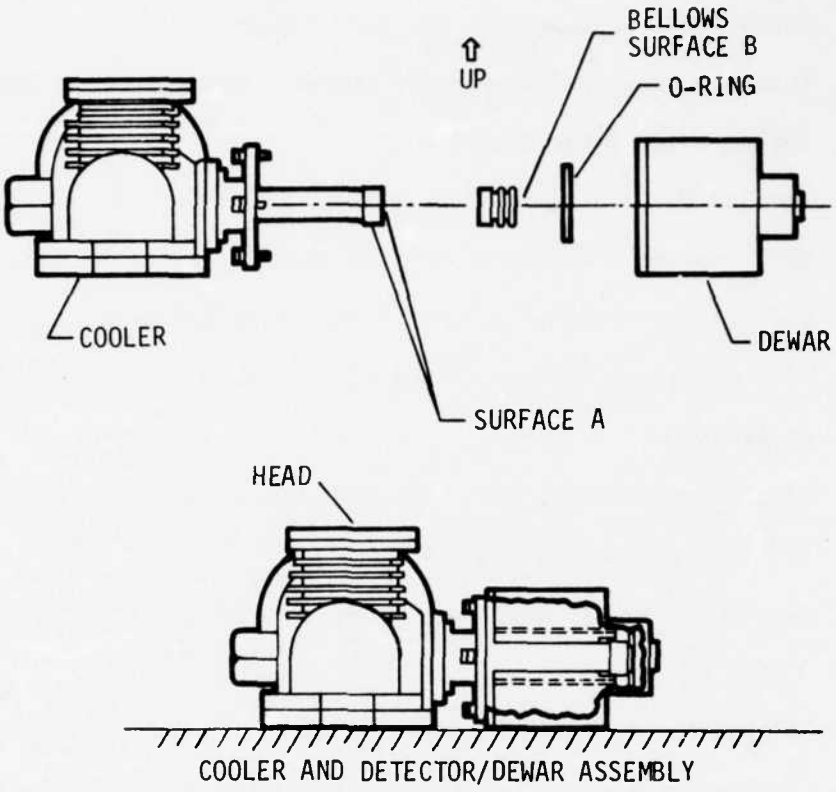


Figure 3.3-16. Cooler and Detector/Dewar Assembly

3.3.3.3.2 Detector/Dewar Vacuum Integrity

A suspect detector/dewar with poor vacuum (and excessive heat loading) cannot be accurately diagnosed while it is mounted to a cooler within a system. Only two measurable operating characteristics are available: detector stem/chip temperature (from current and voltage data of the 2N2222 transistor, for which see section 3.4), and input power to the cooler. These data can be used to diagnose a problem, but not to attribute its cause to either the detector or cooler alone.

The most accurate means of determining vacuum integrity is by a test similar to the one described in the development specification B2-28A050102. The dewar is inverted and is partially filled with liquid nitrogen by care-

fully following the procedure discussed in paragraph 3.3.3.3.3 below. The boil-off rate of nitrogen from the dewar is determined by using a mass flowmeter or an accurate balance scale and a timer. The rate to be used in calculating heat loss is the rate just before final boil-off. (The boil-off rate decreases with decreasing liquid nitrogen level in the dewar.) The heat loss is calculated from: (heat loss ~ watts) = (final boil-off rate ~ gm/min) x (3.3).

The specification requires that the getters be capable of being fired 7 times, although this number may be as many as 20 if a catastrophic vacuum failure has not occurred. The manufacturer usually fires both getters (and also performs the initial bake-out) one time. A typical firing procedure is to immerse the dewar in Freon TF to ensure sufficient cooling of the leads and the dewar shell, then immediately fire both getters sequentially at a current of 2.5 amperes for 1 minute, then at 3.3 amperes for 2.5 minutes. Details of pumping speed and capacity are in drawing SM-C-772743.

3.3.3.3.3 Handling

The detector/dewar is the most easily damaged module in the FLIR system. The detector array is not only expensive but fragile, and the elements of the array are sensitive to static charge buildup. For these reasons, the connector pins of the detector array should never be touched. As a safety precaution, the pins should be provided with a blank connector for periods of shipping and shelf storage.

If laboratory tests require filling the dewar with liquid nitrogen, the following precautions should be observed:

1 When filling, ensure that no water is in the dewar, because this

could cause the dewar to crack.

2 If the nitrogen has boiled off, do not refill with nitrogen until the condensation has evaporated or has been carefully removed with a cottom swab. Keep all other objects out of dewar.

3 When filling a dewar, ensure that the O-ring has been removed from the dewar flange. Liquid nitrogen could degrade the properties of the seal.

4 Use a funnel to fill the dewar and fill only halfway. Spillover could cause the dewar shell to crack because of the expansion properties of the glass-to-metal shield at the top of the dewar.

5 For laboratory testing with a Joule-Thompson cryostat, the use of high pressure nitrogen is preferred over high pressure air to preclude the possibility of dry ice forming from traces of carbon dioxide in the air and clogging the cryostat.

6 When mating a detector/dewar with a cooler, make sure that the bellows will compress easily. Excessive compression force caused by excess thermal grease inside the bellows or by some other foreign substance between the convolutions could break the glass stem.

3.4 Electronics Design

This section provides system electronics considerations, a system interconnect discussion, design recommendations for the system-peculiar power supply, and electrical system alignment and setup procedures. System electronic considerations include a general video electronics description, common module implementation requirements, and video electronics bandwidth and phase lag. Appendix B provides a thorough system noise analysis and

defines special system bandwidth considerations for reference in this section. The system interconnect discussion describes hookup and grounding considerations for the video electronics common modules, cooler, and inverter. A power supply design discussion offers advice on a high-power mode implementation through an example problem. Differences for a low-power implementation are described. Finally, electrical system setup and alignment procedures are included for the video electronics and the scan and interlace module and mechanical scanner module interface. Detailed electrical characteristics of the common modules are provided in Appendix A, sections A.1 through A.8.

3.4.1 System Electronics Considerations

3.4.1.1 General Description

The video electronics block diagram is shown in Figure 3.4-1 for one channel of the video chain, which starts at the input to the detector and terminates at the LED array output. For systems of any size up to 180 channels, only one each of the following modules is required: detector/dewar, bias regulator, auxiliary control, and LED array. Both the preamplifier and postamplifier control driver modules contain 20 channels per module and are cascaded in parallel to fulfill a given systems requirement. When systems of less than 180 channels are used, the center of the LED array and detector/dewar module channels are used first with channels 1 and 180 being the last channels used.

As decribed in paragraph 3.4.2.1, the logical and intended method of channel grouping is in combinations of five channels. Each group of five detectors has one common return which is processed to one preamplifier

integrated circuit (IC) containing five preamplifiers with one common ground. The five outputs of the one preamplifier IC with their common ground are connected to one five-channel postamplifier IC. This approach is continued all the way to the output of the LED driver which also has five amplifiers per IC.

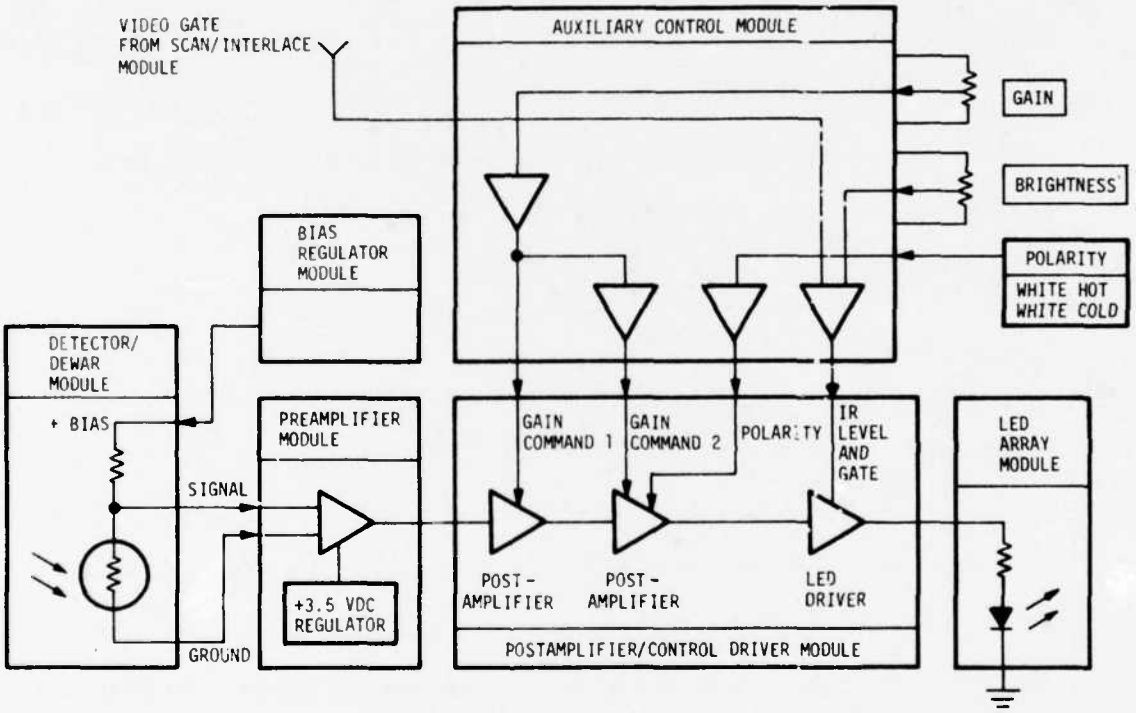


Figure 3.4-1. Video Electronics

The bias regulator module provides a low-noise and low-ripple source to the detector array. The auxiliary control module processes control panel functions such as gain, brightness, and polarity into a form which controls the appropriate amplifiers on the postamplifier/control driver module. This module also accepts a blanking pulse from the scan and interlace module which is ANDed with the IR-level function to blank during interlace time. The preamplifier module is used to amplify the detector

signal while introducing a minimum amount of noise, and the postamplifier/control driver module amplifies the signal to a level necessary to drive the LED array. All video electronics up to and including the first postamplifier are extremely susceptible to ripple and EMI that add unwanted noise at the final display/output.

3.4.1.1.1 Detector/Dewar

The detector elements are implemented in a monolithic array as part of an assembly which includes bias resistors and a self-contained insulating dewar. The elements are biased with a constant current from the bias regulator so that a change in element resistance due to incident IR can be detected as a voltage change at the preamplifier input. The detectors are arranged within the module so that the elements are connected in groups of 45 at the rear of the array. Therefore, four connectors are required to access all 180 elements. Two connectors represent the 90 innermost elements equally spaced about the center, and the other two connectors represent the 90 outermost elements. Within each segment, there is a return for every five detectors and a bias input for every 15 detectors. This implementation permits selective application of power in increments of five detectors so that the array can be tempered for different system applications without unnecessary power dissipation. Each detector is biased with a regulated 5 volts through approximately 2 kΩ bias resistors mounted in groups of 15 which act as current sources. Figure 3.4-2 shows a schematic of one complete segment of the detector array (45 detectors).

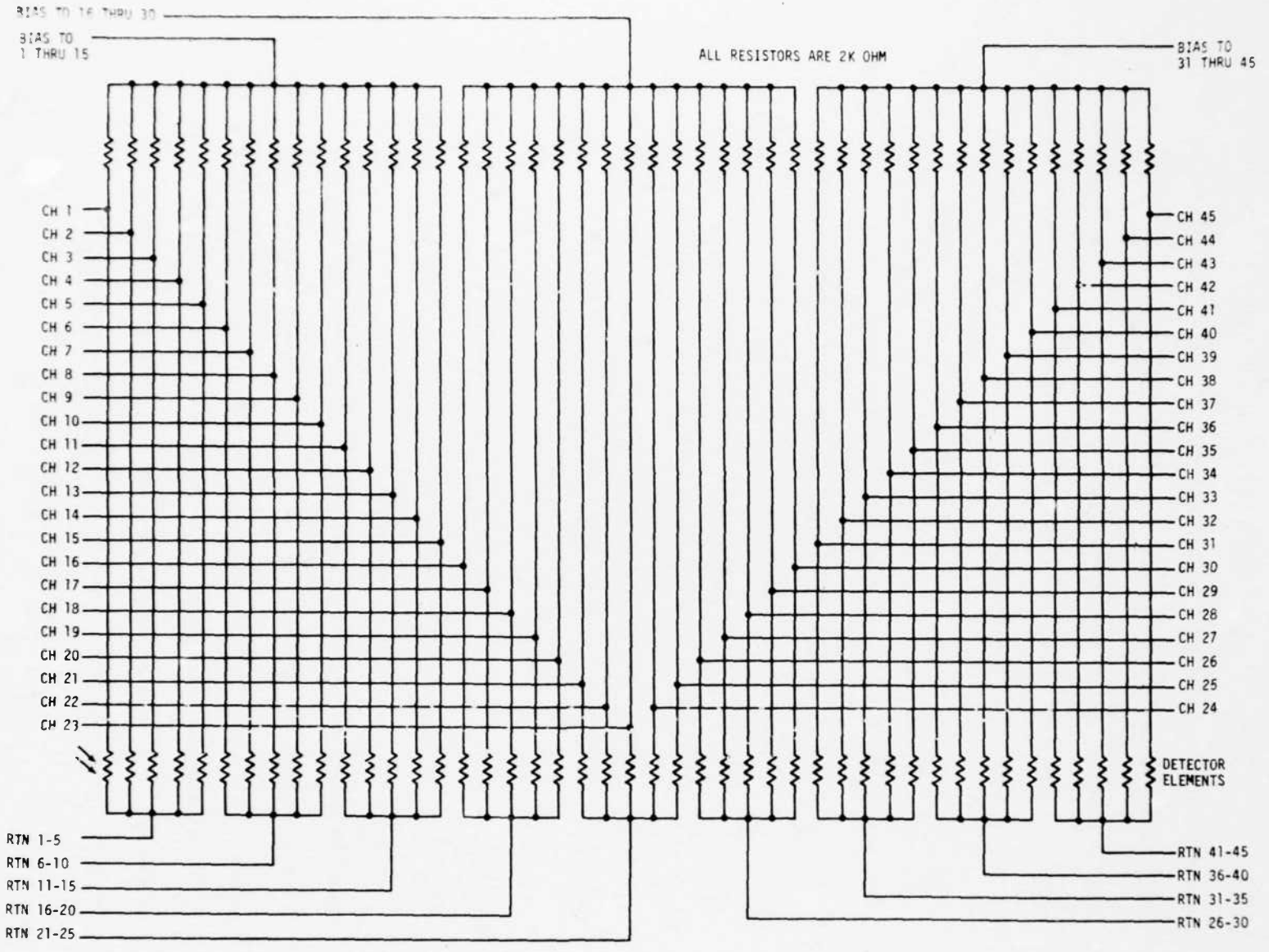


Figure 3.4-2. Detector Array Typical Arrangement

A temperature sensor is also incorporated within the detector/dewar module. This sensor is the base-emitter diode of a 2N2222A transistor which uses the temperature dependence of V_{BE} for sensing. Empirical data indicate forward voltage ranges are from 1.06 Vdc at 77°K to 0.7 Vdc at room temperature. One sensor is placed in each of the two center sections of the array and are for use primarily with systems where particular temperature levels of the detector are to be monitored. A diode voltage versus temperature calibration is supplied with each module.

3.4.1.1.2 Preamplifier

3.4.1.1.2.1 Implementation

Each preamplifier module contains circuitry as shown in the block diagram of Figure 3.4-3. The amplifiers are ICs with a density of five amplifiers (channels) per IC package. The amplifiers are low-noise and require the use of the +3.5 Vdc regulator, as shown, to reduce the ripple of the power supply to a level which is acceptable for a low-noise system. The amplifiers are ac coupled at both the input and output. An option is provided that permits the user to bypass the on-board +3.5 Vdc regulator when power supply ripple rejection is not required, thus permitting the design of a more power-efficient system. This option should be reserved for those systems that use a low-noise source as the supply voltage to the preamplifier module, such as a battery.

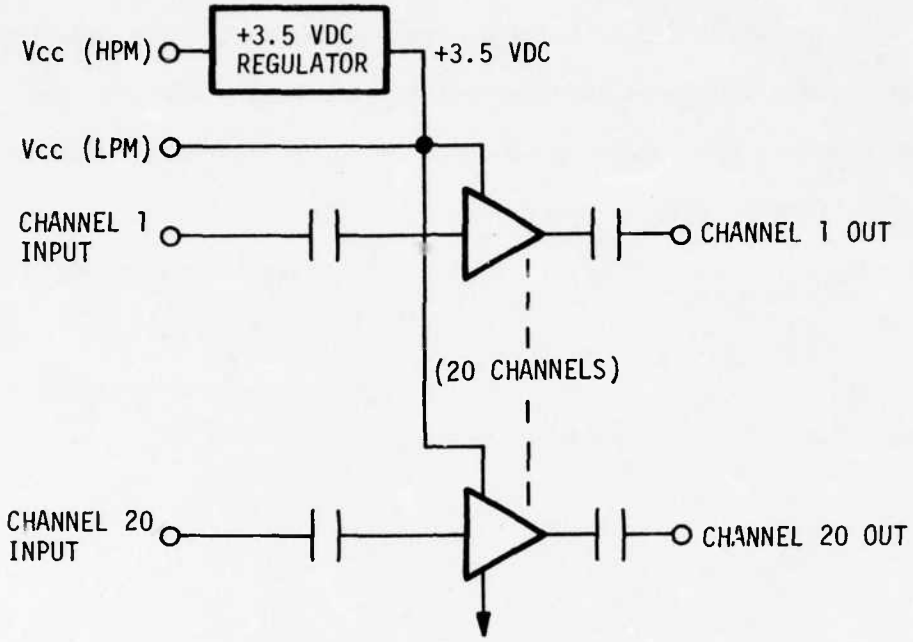


Figure 3.4-3. Preamplifier

3.4.1.1.2.2 +3.5 Vdc Preamplifier Regulator dc Output Voltage Considerations

A schematic of the preamplifier module is shown in Figure 3.4-4. The regulator is the circuitry above AR1. The +3.5 Vdc output is determined primarily by the V_{BE} of Q3 and the zener voltage of CR3 which has a very soft knee ($V_o = V_{BE3} + V_{CR3}$). This factor contributes heavily to the broad range of the regulator output voltage tolerance of +36 percent which is specified in Table 3.4-I. The increase in output voltage becomes significant only in a low input voltage mode when the voltage across Q1 decreases to a point where Q1 saturates. The output voltage might appear regulated during this mode but all power supply rejection of the regulator is lost when Q1 saturates and the amplifier becomes nonlinear, thus coupling all power supply ripple directly to the V_{CC} input of the preamplifier.

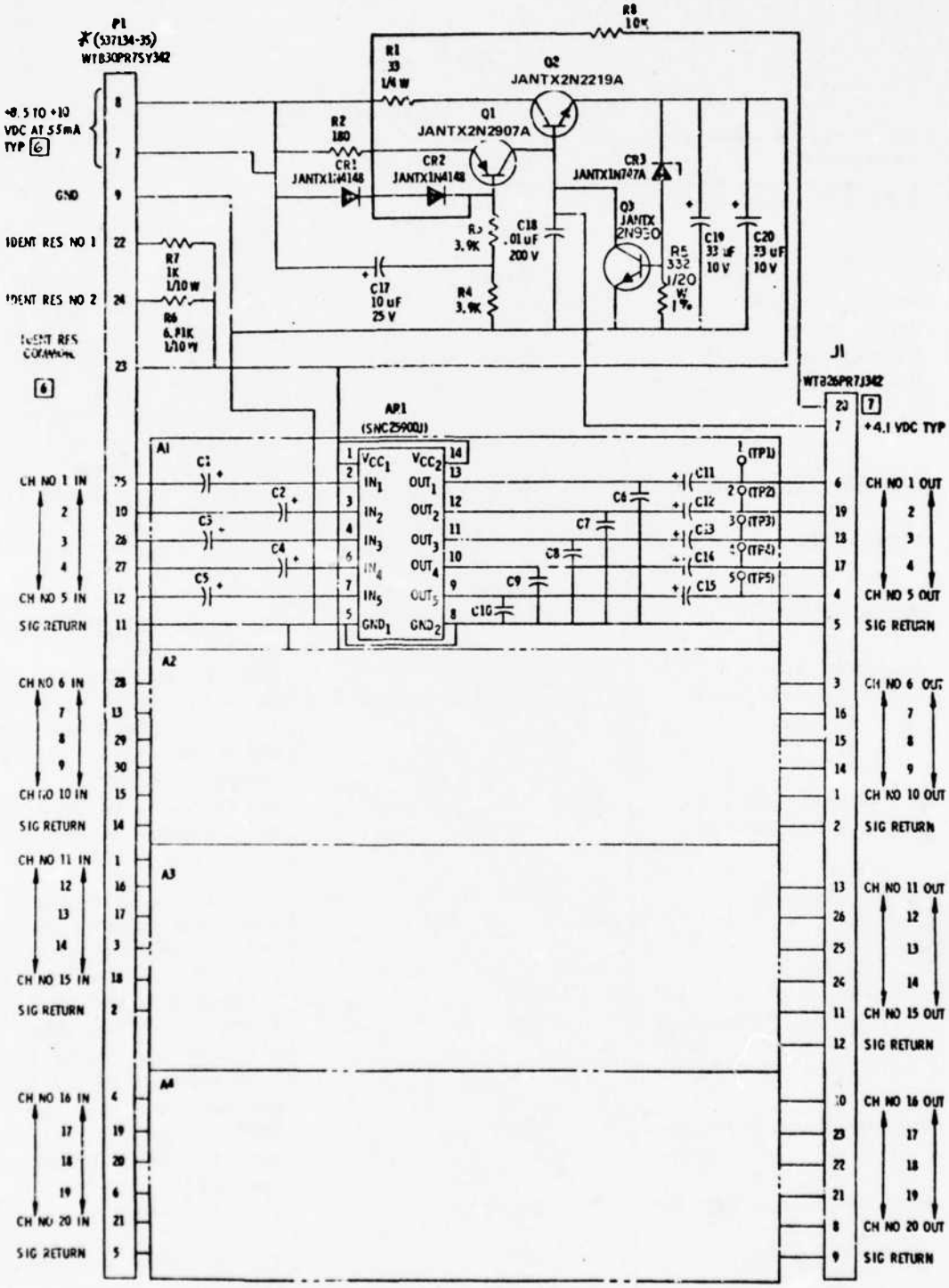


Figure 3.4-4. Video Preamplifier Schematic

TABLE 3.4-I

Preamplifier Characteristics

Parameter	Characteristics	Comments
Supply Voltage (Vdc)	3.0 ± 0.3	LP mode
	9.25 ± 0.75	High-power(HP) mode
Supply Current (mA)	44 ± 5	LP mode
	55 ±6	HP mode
Voltage Gain*	70 ±7 V/V	ac gain; no dc gain
Input Impedance*	4.0 - 6.5 kΩ	ac measured @ 1 kHz
Output Impedance*	0.4 - 0.75 kΩ	ac measured @ 1 kHz
Maximum Input Signal*	0.01 Vrms	LP mode; @ kHz; less than ±5% harmonic distortion as recorded on a distortion analyzer
Low-Frequency Cutoff*	1.06 ±0.45 Hz†	-3 dB from voltage gain @ 1 kHz
High-Frequency Cutoff*	105 ±25 kHz	-3 dB from voltage gain @ 1 kHz
	120 ±44 kHz†	
Flatness	±0.5 dB	30 Hz to 30 kHz; reference @ 1 kHz
Recovery Time*	0.2s	See section 3.4.1.1.2.4
White Noise* (rms)	1.5×10^{-9} V $(Hz)^{-1/2}$	Bandwidth determined by low and high frequency break points of channel being measured
1/f Noise* (rms)	10×10^{-9} V $(Hz)^{-1/2}$	Bandwidth = 10 Hz @ 100 Hz
Channel Crosstalk	-30 dB	19 channels into 1 @ 1 kHz, e_{in} = 1.4 mV
Noise Figure	5.7 dB	Rs = 10 kΩ; (requires equivalent input noise voltage of the amplifier to be 0.7 μV for a signal bandwidth = 100 kHz)
Voltage Gain Tracking	±5%	-54°C to +71°C; channel voltage gain variation from average of 20 for the module
Voltage Gain Drift	±10%	-54°C to +71°C; voltage gain tracking variation from 25°C
+3.5 Regulator Ripple Rejection	60 dB†	0 to 100 kHz
+3.5V Regulation	-2%†	-55 to 95°C; and end-of-life
	+36%†	

*Each one of the 20 channels
†By analysis

3.4.1.1.2.3 Preamplifier Regulator Low-Power (LP) Mode Considerations

For uses concerning the LP mode, such as a battery source for the V_{CC1} supply of the preamplifier, the +3.5 Vdc regulator is not used. In this mode, the source is connected directly to pin 23 of the module. It is important to note that the voltage at pin 23 should be held to less than 3.3 Vdc as specified to ensure that CR3 does not sink too much current (power inefficiency) and/or fail catastrophically. Also, as specified in Table 3.4-I, the minimum voltage should be held to 2.7 Vdc or greater. Below this level, the preamplifier IC is not guaranteed to perform as specified.

3.4.1.1.2.4 Recovery Time

The recovery time is specified at 0.2 second to ensure that a high-intensity signal such as a projectile followed by a low-intensity signal (target) can be seen. The input signal to the preamplifier is as shown in Figure 3.4-5. Analysis for the preamplifier and complete video chain demonstrates that this requirement can be met.

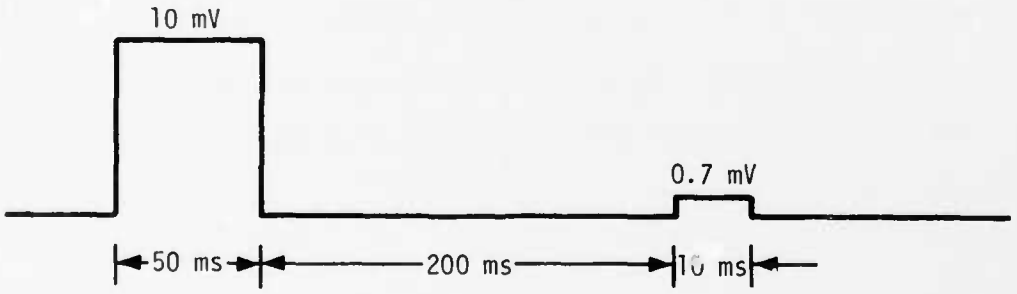
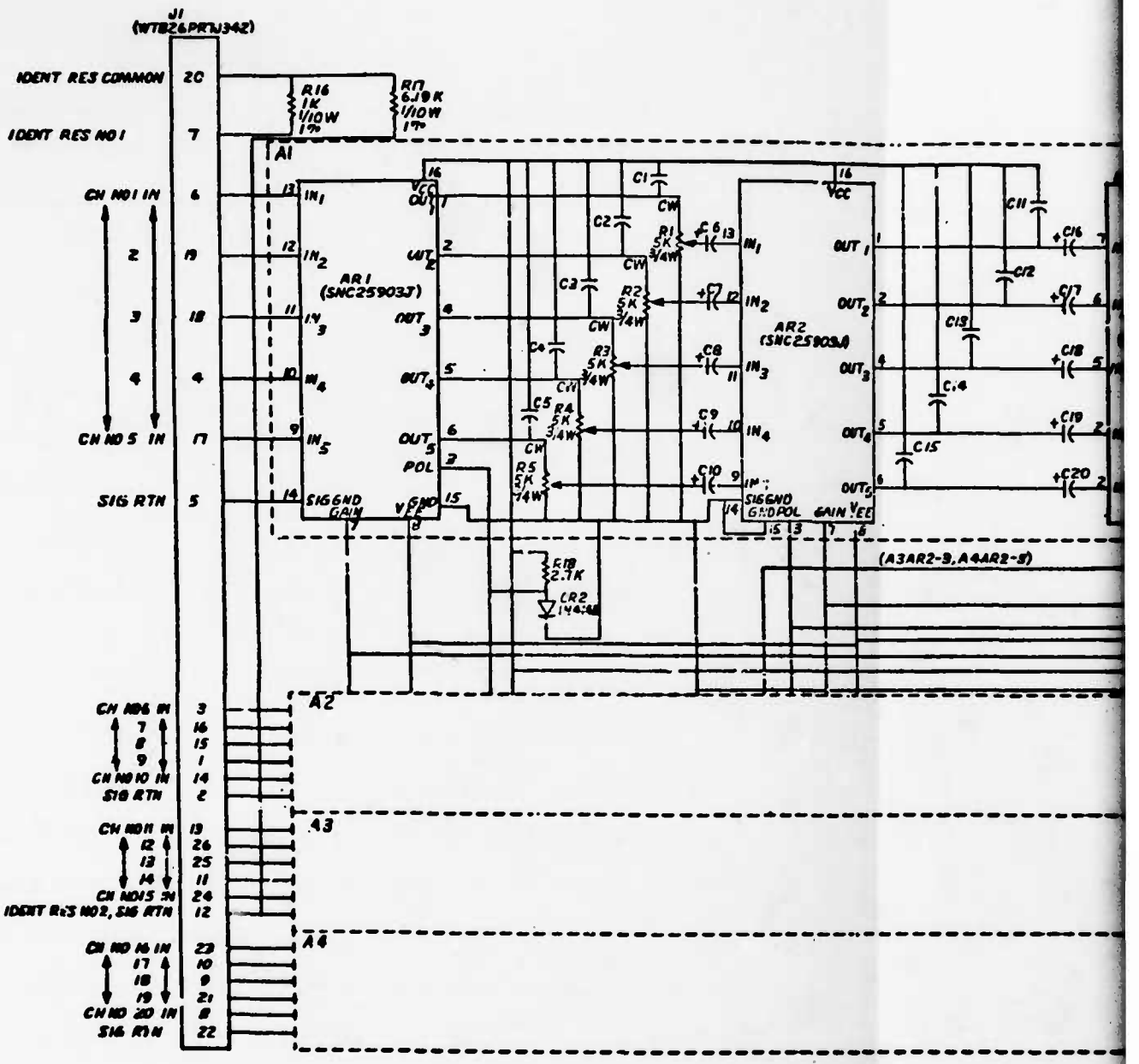


Figure 3.4-5. Recovery Test Input Signal

3.4.1.1.3 Postamplifier/LED Driver

The block diagram described in section 3.4.1.2 shows the circuitry that makes up one complete channel out of the 20 on the postamplifier module. There are five postamplifiers per IC package and five LED drivers per IC package. The complete module schematic is shown in Figure 3.4-6. Each channel contains two postamplifiers and one LED driver in series, with a potentiometer in each channel to control the initial gain. Each postamplifier has a voltage-controlled gain command input for a 30 dB contrast control and a polarity input that permits the selection of white hot or white cold. Each LED driver has a brightness level input that allows setting of the output dc level of the LED driver which in turn sets the quiescent current through the LED and consequently the brightness. The module has two basic power supply modes, one is a HP mode and the other a LP mode where system efficiency can be increased at the expense of such system parameters as decreased run time (because a battery is used) and/or LED brightness and dynamic range. The module is intended to process video signals in the 7 Hz to 70 kHz range and can provide a minimum programmable gain in the range of 80 to 85 dB (10,000 to 18,000).

The auxiliary control module described in section 3.4.1.1.4 provides voltages and controls to the postamplifier/control driver module as described in Table 3.4-II.



REF. DES.	VALUE	VOLTAGE
C1-C5	4700 pf	100 V
C6-C10	4.7 mf	35V
C11-C15	390 mf	200V
C16-C20	4.7 mf	35V
C21-C25	390 pf	200V
C26-C28	10 mf	20V
C29-C30	33 mf	10V

TABLE 1

PI PINS	LOW POWER SYSTEM SUPPLY VOLTAGE	HIGH POWER SYSTEM SUPPLY VOLTAGE
32	+6.5 VDC	+6.5 VDC
17	+4.8 VDC	+10 VDC
2	+4.8 VDC	+10 VDC
29	+4.8 VDC	+10 VDC
18	-4.8 VDC	-6.5 TO -7.4 VDC
30	+7 VDC	DISCONNECTED
27	-9.5 VDC	-4.25 VDC
11	+9.5 VDC	+4.25 VDC

TABLE 2 NOMINAL VOLTAGES

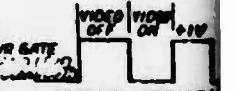
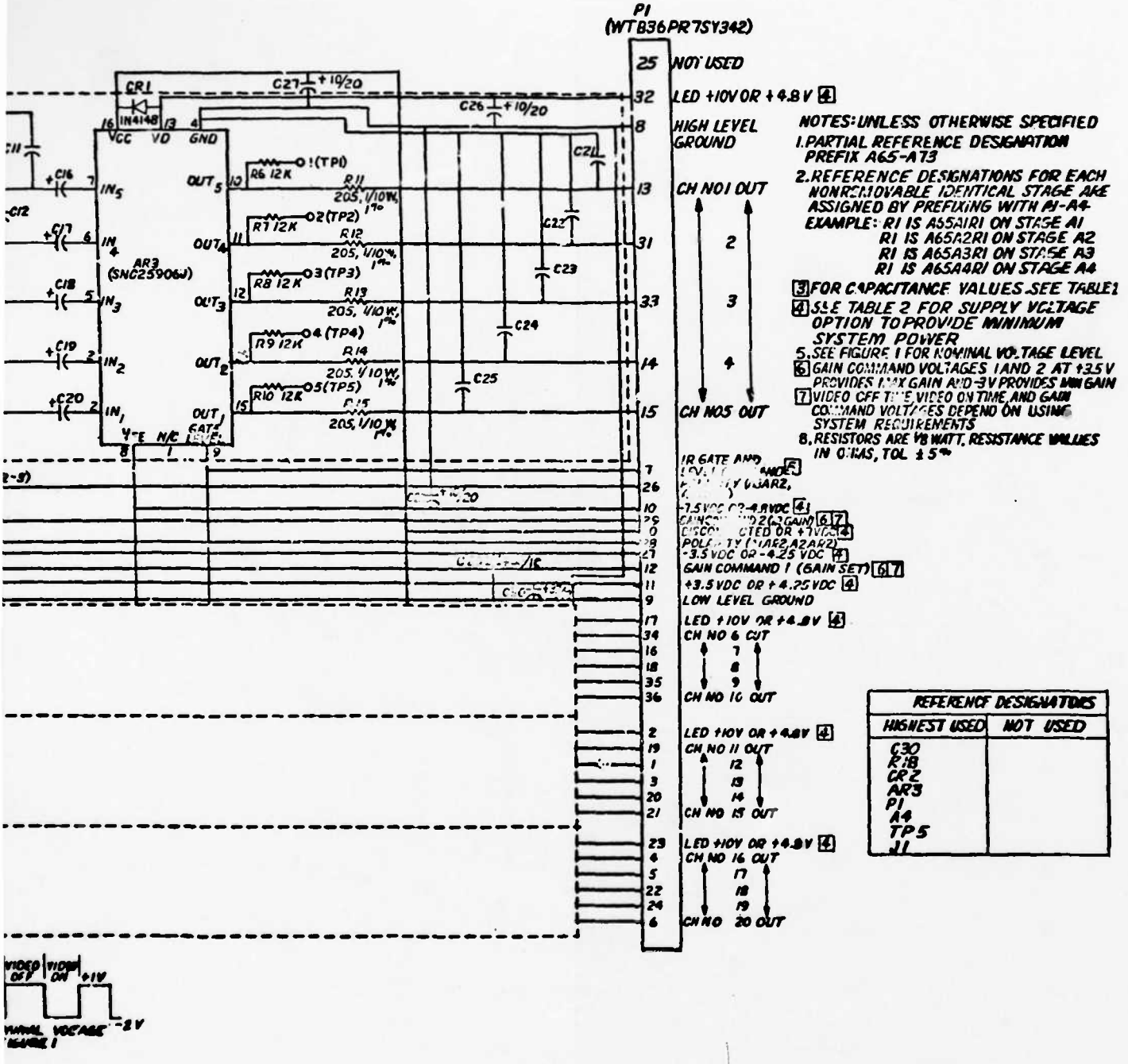


FIGURE 1



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATION PREFIX A65-A73
2. REFERENCE DESIGNATIONS FOR EACH NONREMOVABLE IDENTICAL STAGE ARE ASSIGNED BY PREFIXING WITH P1-A4
   EXAMPLE: R1 IS A65A1R1 ON STAGE A1
   R1 IS A65A2R1 ON STAGE A2
   R1 IS A65A3R1 ON STAGE A3
   R1 IS A65A4R1 ON STAGE A4
3. FOR CAPACITANCE VALUES SEE TABLE1
4. SEE TABLE 2 FOR SUPPLY VOLTAGE OPTION TO PROVIDE MINIMUM SYSTEM POWER
5. SEE FIGURE 1 FOR NOMINAL VOLTAGE LEVEL
6. GAIN COMMAND VOLTAGES 1 AND 2 AT +3.5 V PROVIDES MAX GAIN AND -3V PROVIDES MIN GAIN
7. VIDEO OFF TIME, VIDEO ON TIME, AND GAIN COMMAND VOLTAGES DEPEND ON USING SYSTEM REQUIREMENTS
8. RESISTORS ARE 1/8 WATT, RESISTANCE VALUES IN OHMS, TOL ± 5%

REFERENCE DESIGNATORS	
HIGHEST USED	NOT USED
C30	
R18	
CR2	
AR3	
P1	
A4	
TP5	
J1	

Figure 3.4-6 Postamplifier/Control Driver Schematic

TABLE 3.4-II

Postamplifier/Control Driver Voltages and Controls

Input	Module Pin Number	Amplifier Pin Number	Comments
Positive Regulator	11	AR1, AR2, P16	+3.5 to +4.25 Vdc
Negative Regulator	27	AR1, AR2, P8	-3.5 to -4.25 Vdc
Polarity	28	A1, A2 of AR2, P3	Pins 28 and 26 of module
	26	A3, A4 of AR2, P3	Connected together normally
IR Gate and Level	7	AR3, P9	Brightness and blanking
Gain Command 1	12	AR1, P7	-3.0 to +3.0 Vdc nominal
Gain Command 2	29	AR2, P7	0.0 to +0.5 Vdc nominal

The positive and negative regulator inputs provide power to the postamplifier only, while the LED drivers are supplied power on pins 2, 10, 17, 23, 30, and 32. For the HP mode, pins 2, 17, 23, and 32 are connected to +10 Vdc, pin 10 to -7.5 Vdc, and pin 30 is open; while pins 11 and 27 are connected to +4.25 Vdc and -4.25 Vdc, respectively. For the LP mode, pins 2, 17, 23, and 32 are connected to +4.8 Vdc, pin 10 is connected to -4.8 Vdc, and pin 30 is connected to +7 Vdc or greater; while pins 11 and 27 are +3.25 Vdc and -3.25 Vdc, respectively. These values of voltages are the recommended values and any deviations therefrom should be considered only after the IC specifications are reviewed.

Polarity is a function connected to the second postamplifier on the module. The first postamplifier is always biased in the inverting mode by the positive potential of CR2, which is connected to the AR1 polarity

input at pin 3. When the polarity input is +0.6 ±0.25 Vdc, the second postamplifier is operating in the inverting mode. When the polarity input is -3.5 ±1.5 Vdc, the second postamplifier is operating in the noninverting mode. For normal system operation using the configuration discussed in paragraph 3.4.2.4, white hot requires a +0.6 Vdc input on the polarity input.

The IR gate and level input (pin 7 of the module) is a positive voltage level (+1 Vdc) when the output signal from the LED driver is to be blanked. For variable brightness levels, the magnitude of the input varies between the limits from 0 to -1.5 Vdc. The gain from the gate level input of AR3 (pin 9) to the IC output (pins 10, 11, 12, 14, and 15) is approximately 6 V/V. The IR gate and level input is normally a variable-duty-cycle, rectangular waveform with the negative level occurring during the scan time and the +1 Vdc occurring during interlace time as described in paragraph 3.4.1.1.4. Postamplifier and LED driver IC characteristics are provided in Appendix A.3. This appendix also contains the results of measurements performed to further establish characteristics potentially important in system applications.

3.4.1.1.4 Auxiliary Control

A schematic of an auxiliary control module is shown in Figures 3.4-7 and 3.4-8. The circuitry shown in Figure 3.4-8 represents the +3.5 Vdc and -3.5 Vdc regulator which supplies a low-noise, low-ripple voltage to the postamplifier ICs on the postamplifier/control driver module. Figure 3.4-8 shows the circuitry that accepts control functions and converts them to the necessary form to control brightness, contrast, polarity, and blanking on the postamplifier/control driver module. In addition, there is circuitry

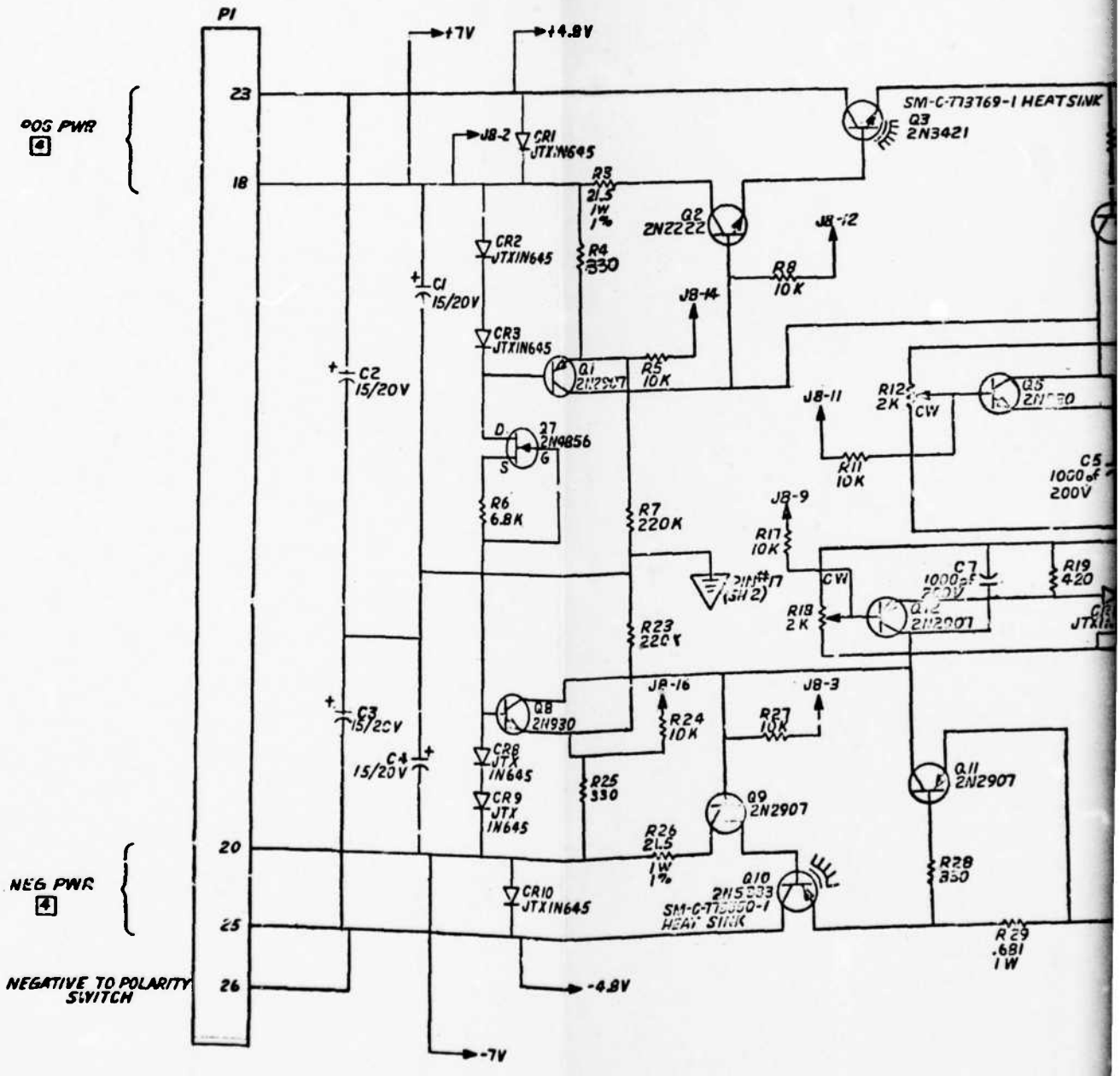
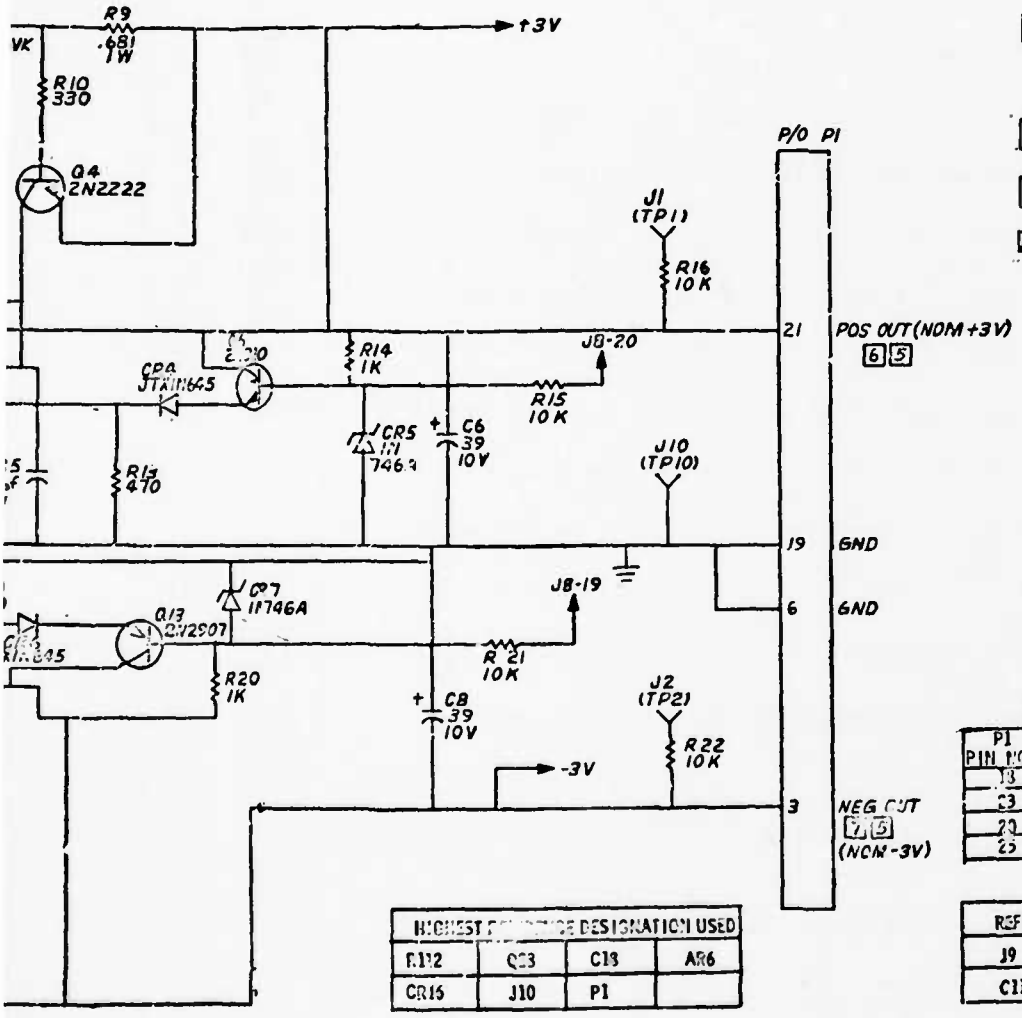


Figure 3.4-7. Positive and Negative Regulators Schematic (Auxiliary Control)

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATION PREFIX A74
2. RESISTORS ARE 1/8 WATT. RESISTANCE VALUES ARE IN OHMS
3. CAPACITANCE VALUES ARE IN MICROFARADS
4. SEE TABLE I FOR SUPPLY VOLTAGE. OPTION TO OBTAIN MINIMUM SYSTEM POWER
5. GAIN COMMAND VOLTAGES IR LEVEL AND GATE LIMITS, GATE PERIOD, AND POS AND NEG REGULATOR OUTPUT VOLTAGES DEPEND ON USING SYSTEM REQUIREMENTS
6. POS REGULATOR OUTPUT VOLTAGE ADJUSTED BY R12
7. NEG REGULATOR OUTPUT VOLTAGE ADJUSTED BY R18
8. SEE WAVEFORMS FOR NOMINAL POLARITY COMMAND VOLTAGES

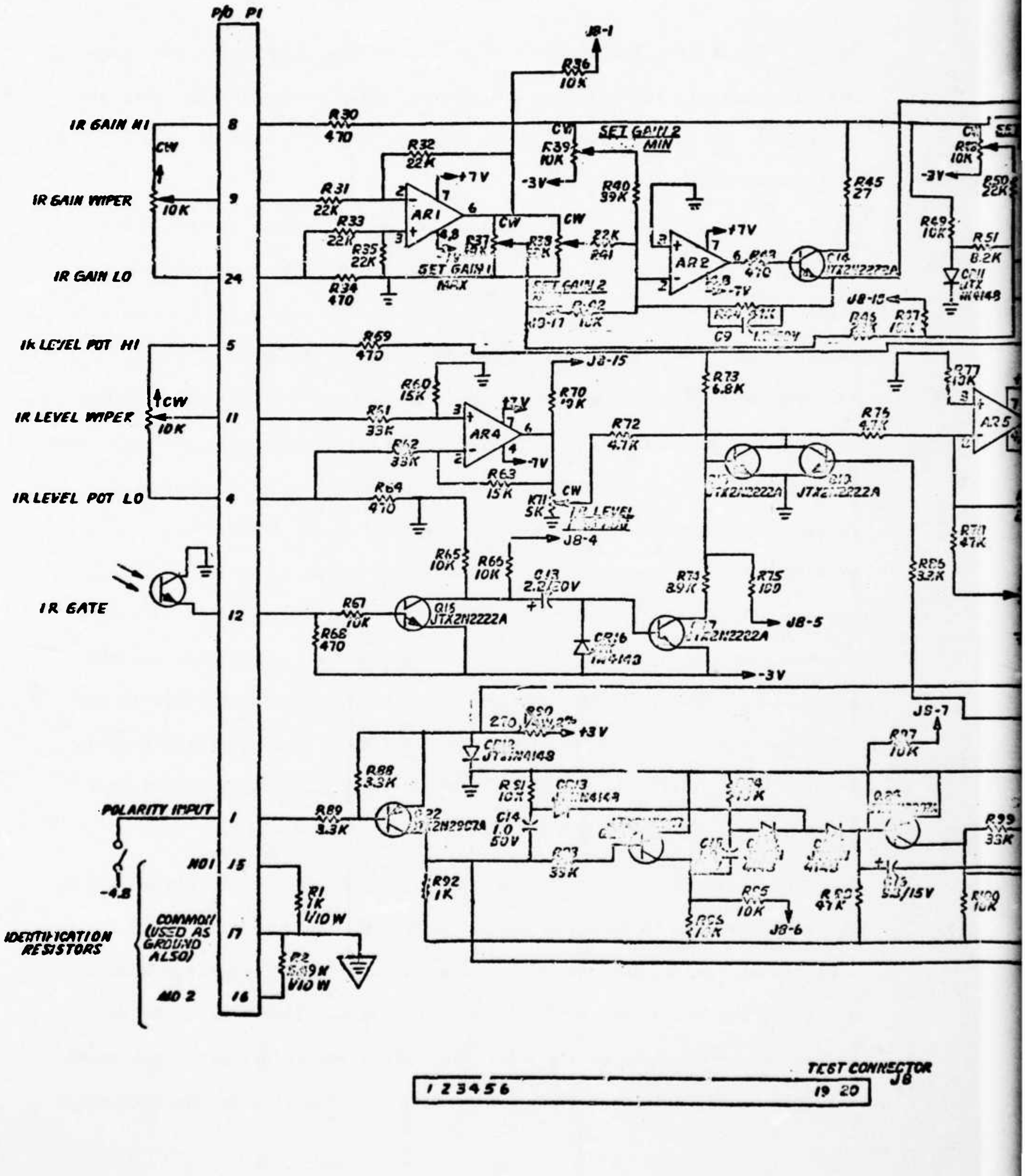


4 TABLE I - NOMINAL VOLTAGES

P1 PIN NO	LOW POWER SYSTEM SUPPLY VOLTAGE	HIGH POWER SYSTEM SUPPLY VOLTAGE
23	+5 VDC	NC
23	+4.8 VDC	+10 VDC
20	-7 VDC	-7.5 VDC
25	-4.8 VDC	-7.5 VDC

HIGHEST REFERENCE DESIGNATION USED			
R112	Q23	C18	AR6
CR16	J10	P1	

REFERENCE DESIGNATIONS NOT USED			
J9	R57	R58	R69
C11	C12		


P/O P1
IR GAIN HI
IR GAIN WIPER
IR GAIN LO
IR LEVEL POT HI
IR LEVEL WIPER
IR LEVEL POT LO
IR GATE
POLARITY INPUT
-4.8
NO1
COMMON (USED AS GROUND ALSO)
IDENTIFICATION RESISTORS
NO 2
J8-1
R36 10K
R30 470
R32 22K
R31 22K
R33 22K
R35 22K
R34 470
AR1
AR2
AR4
AR5
SET GAIN 1 MAX
SET GAIN 2 MIN
R39 10K
R40 39K
R45 27
R69 470
J8-15
R60 15K
R61 33K
R62 33K
R63 15K
R64 470
R70 10K
R72 4.7K
R73 6.8K
R76 4.7K
R77 10K
R78 47K
R85 3.2K
JTX2N2222A
J8-4
R65 10K
R66 10K
R67 10K
R68 470
Q15 JTX2N2222A
C13 2.2/20V
CR16 1N4148
R74 8.9K
R75 100
J8-5
-3V
+3V
J8-7
R97 10K
R88 3.3K
R89 3.3K
R92 1K
R93 33K
R95 10K
J8-6
R99 33K
R1 1K 1/10 W
TEST CONNECTOR J8
1 2 3 4 5 6
19 20

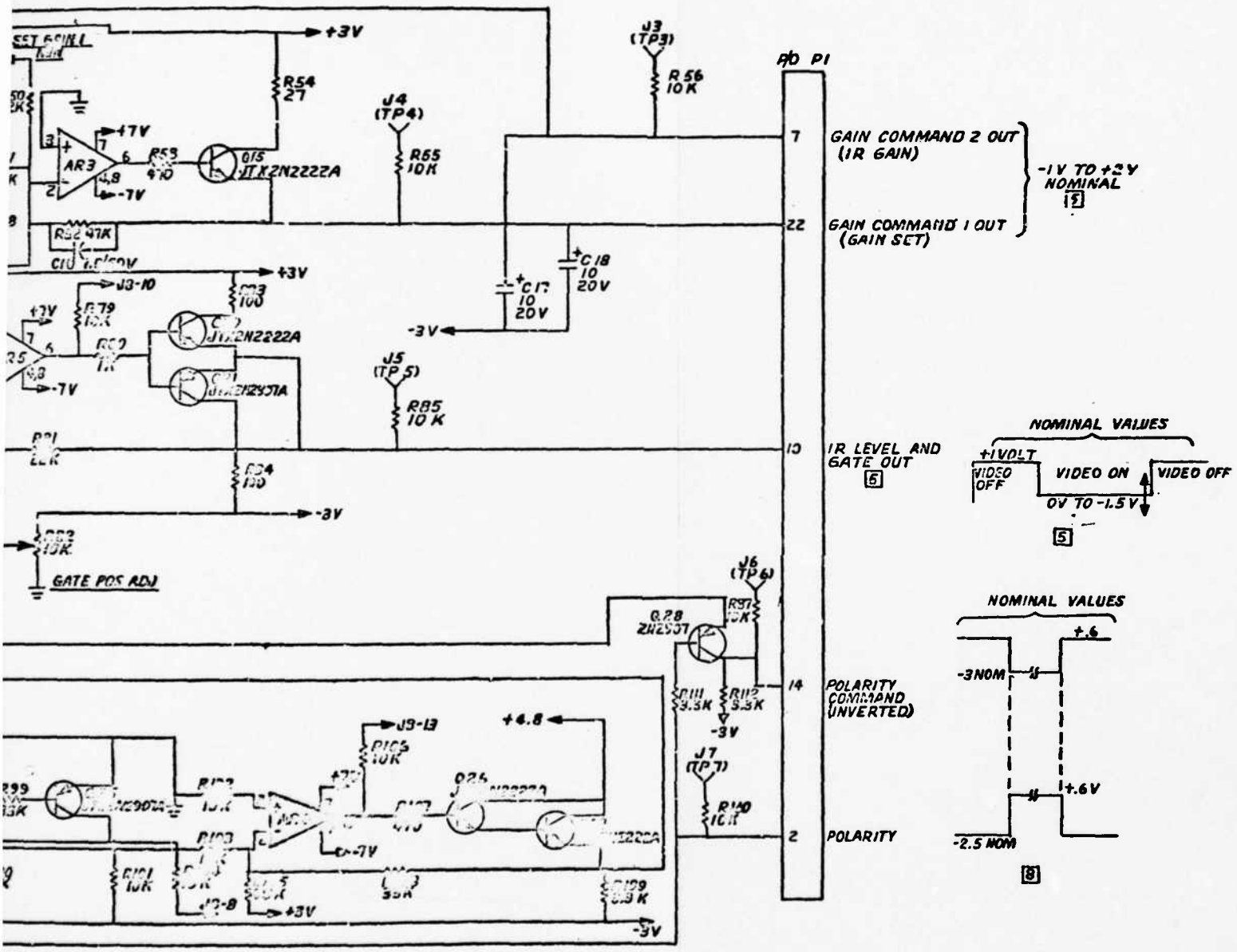


Figure 3.4-8. Auxiliary Control Schematic Control Functions

in the polarity section of the module that forces blanking of the video for approximately 140 ms after a change in the polarity state. This prohibits such potential conditions as blooming when the FLIR is used in conjunction with a TV system.

The contrast function is provided for on the module by the IR-level circuitry and is represented by the gain command 1 and gain command 2 outputs. When the IR-level control potentiometer is varied from one extreme to the other, the outputs can be varied between the limits of -3.0 to +3.0 Vdc on both gain command outputs. These levels may be adjusted by the on-board potentiometers to provide for gain command voltages that permit gain control over a minimum 30 dB range depending on the particular requirements of a system. The nominal range for gain command 1 is -3.0 to +3.0 Vdc while gain command 2 ranges from 0.0 to +0.5 Vdc for a typical system. Although not specified, the gain command 1 output has a positive temperature coefficient of 11 mV/°C. This gradient compensates for the gain versus temperature characteristics of the two postamplifiers of the postamplifier/control driver module and permits a quasi-temperature gain control which maintains the video electronics gain fairly constant over temperature. This is discussed in detail in section A.3.1.

The IR-level circuitry is represented by AR4 and AR5 in Figure 3.4-8. The output at pin 10 is a rectangular waveform, the duty cycle of which is a representation of the scan time. When the positive level is approximately 0.6 volt, the LED driver amplifier of the postamplifier/control driver module causes blanking of the LEDs. When the level is negative, the brightness of the LED driver is being controlled as a function of the setting of

the potentiometer at input pin 11. The scan rectangular waveform is generated by the scanner to represent the scan time and is connected to pin 12 of the module. The absence of this signal causes a blanking signal to appear continuously at output pin 10.

The polarity input provides an output that is approximately +0.6 volt or -3.5 volts and provides for the inversion of the signal in the video chain by controlling the polarity of the second postamplifier of the postamplifier/control driver modules. The circuitry immediately to the right of the pin 1 polarity input is a dual-triggered one-shot that blanks the IR-level output during any change in state of the polarity switch.

A test point is provided (J8-5) which disables blanking when grounded. This makes it possible to measure video noise at the postamplifier output for the NEΔT test.

3.4.1.1.5 Bias Regulator

The bias regulator module, which consists of one printed circuit board, provides a low-noise, low-ripple bias to the 180 detector elements of the detector/dewar module. The schematic of the bias regulator is shown in Figure 3.4-9.

Of primary interest are the ripple rejection and noise characteristics of the regulator that are discussed in Appendix B. These results demonstrate that the attainable ripple at the input to the bias regulator should be held to less than 2 mVrms.

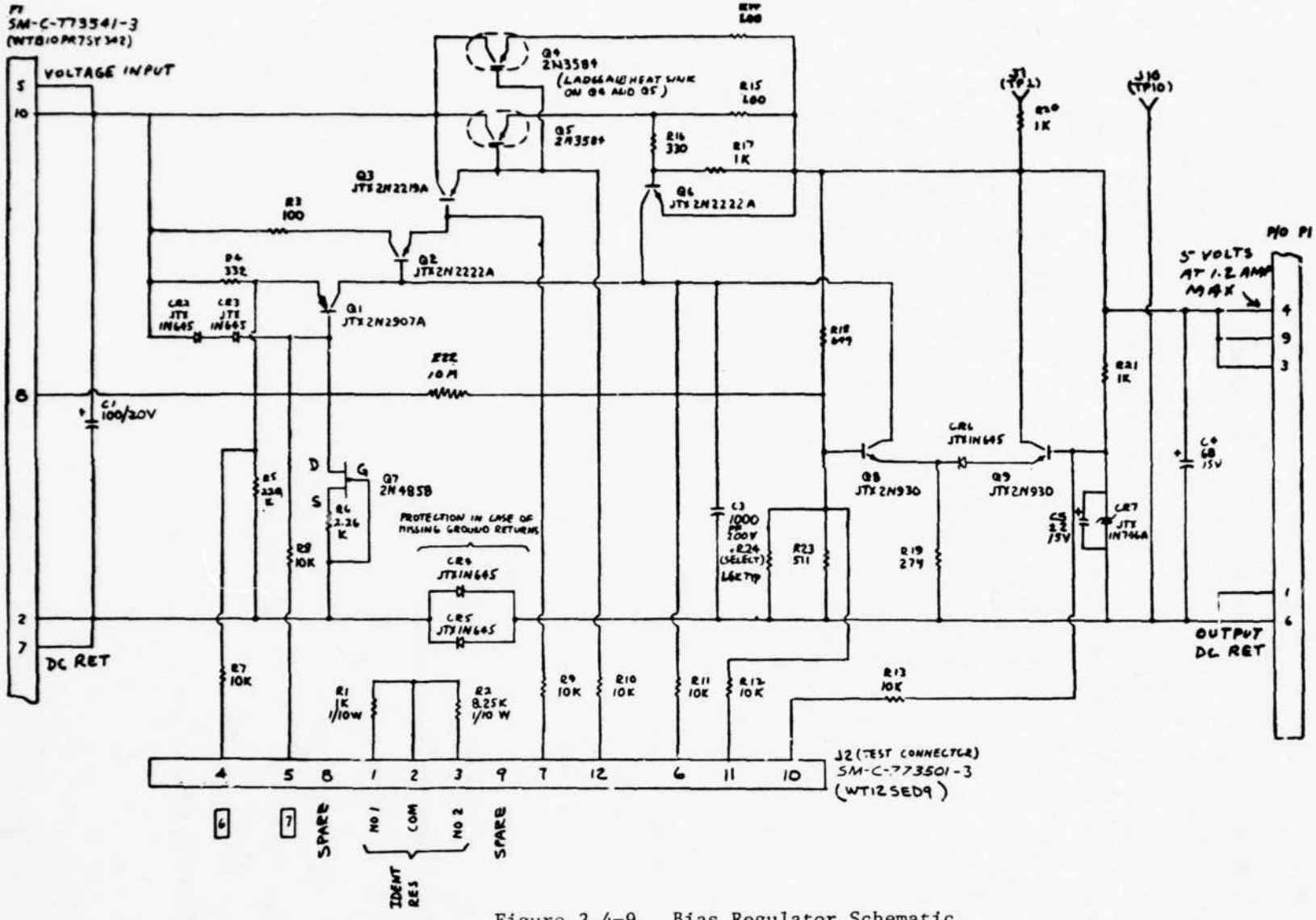


Figure 3.4-9. Bias Regulator Schematic

3.4.1.1.6 Scan and Interlace

The scan and interlace module provides the circuitry to control the scan mirror located within the mechanical scanner module. The circuitry (Figure 3.4-10) provides the following basic functions: scan position control loop, transducer gain regulator loop, interlace position control loop, and the external synchronization loop.

The scan position loop shown in Figure 3.4-11 controls the azimuth position of the mirror, the interlace loop controls the tilting of the mirror to provide interlacing of adjacent scans, the transducer gain loop provides a regulated voltage to the transducer bridge circuitry to maintain its output constant with transducer gain variations, and the synchronization loop adapts the scan position and interlace loops to that of an external source. Appendix A.6 provides a description of the scan position control loop, transducer gain regulator loop, interlace position control loop, and a summary of module characteristics.

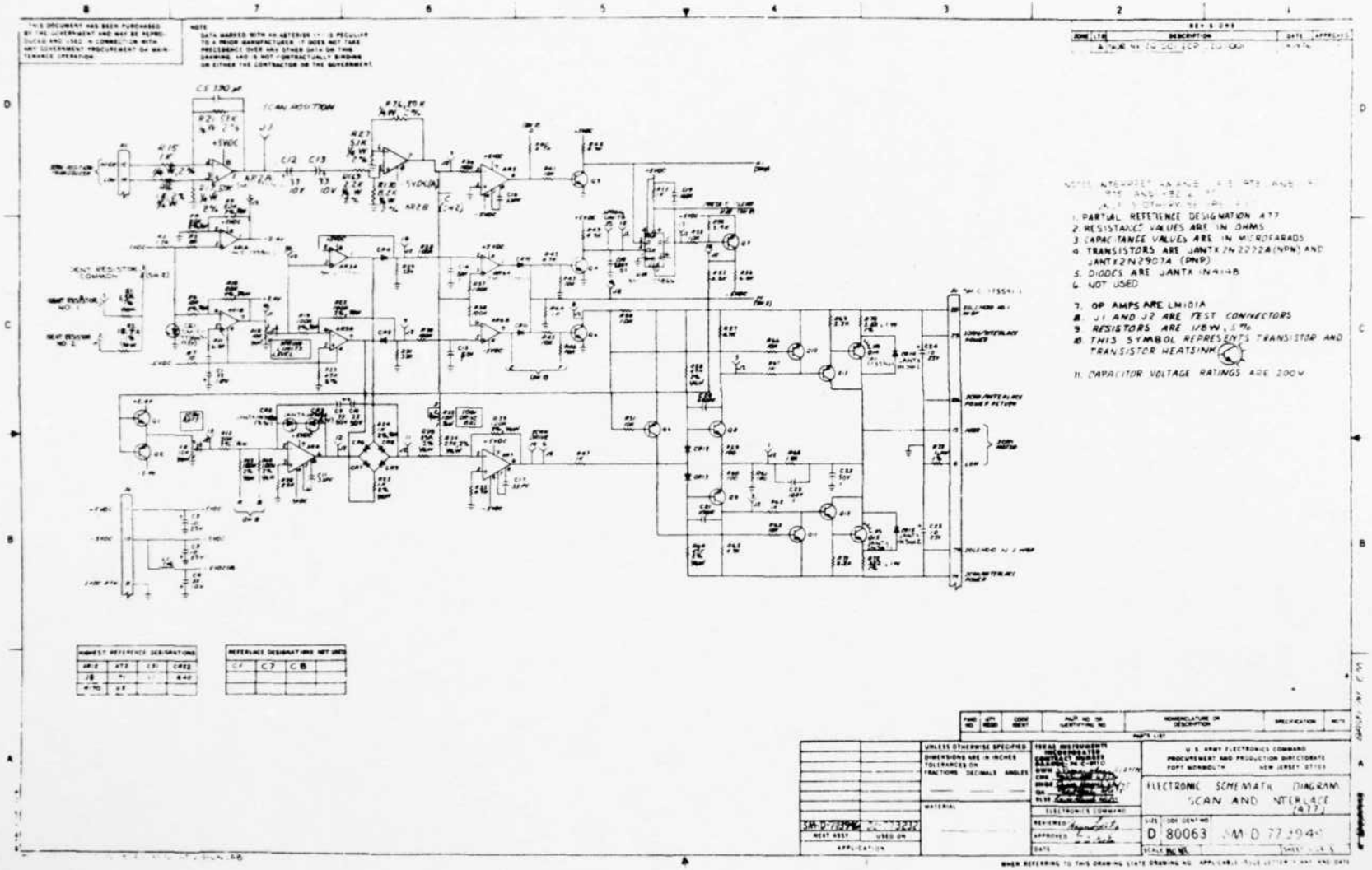


Figure 3.4-10. Scan and Interlace Schematic

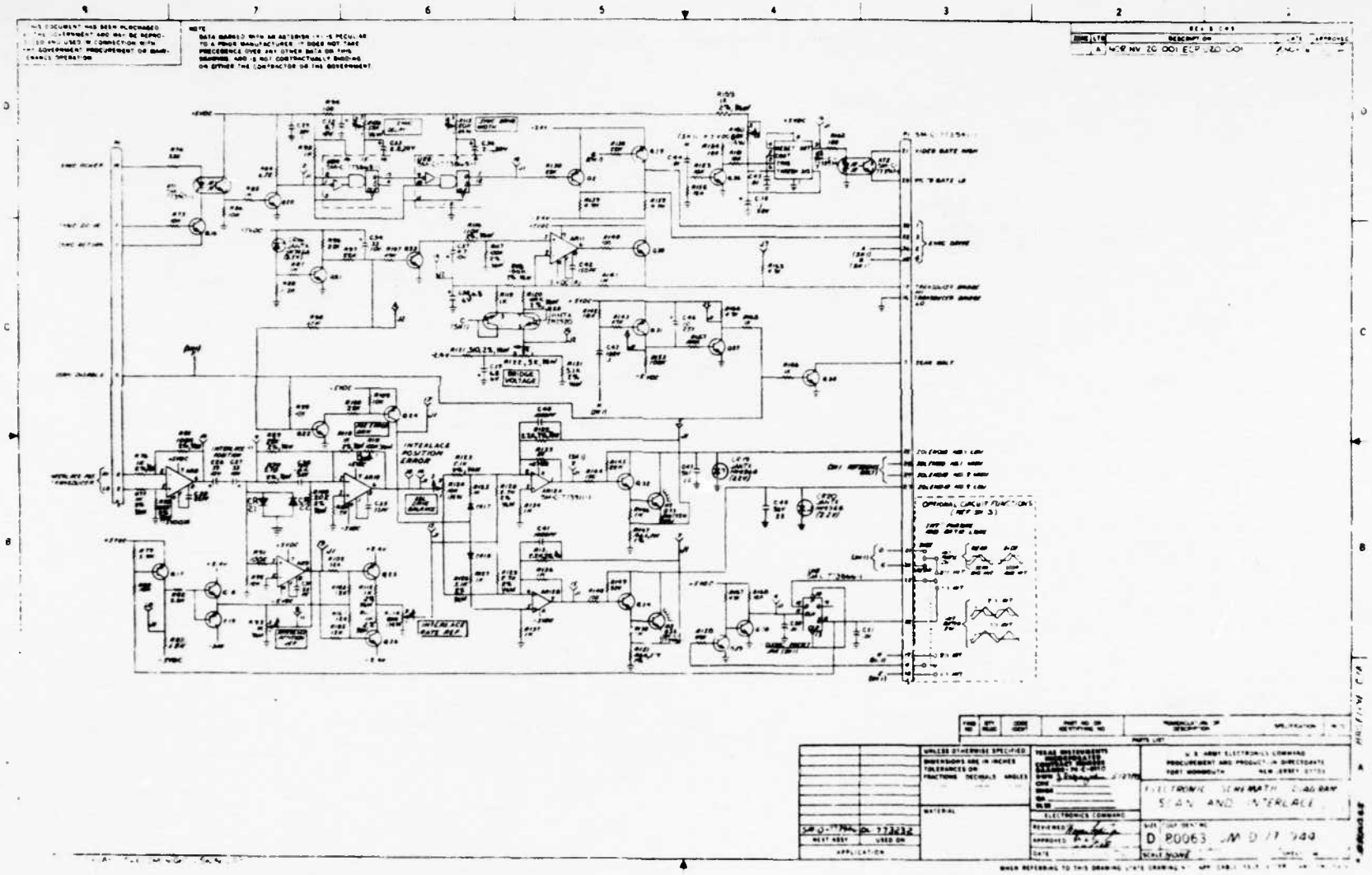


Figure 3.4-10. (Cont)

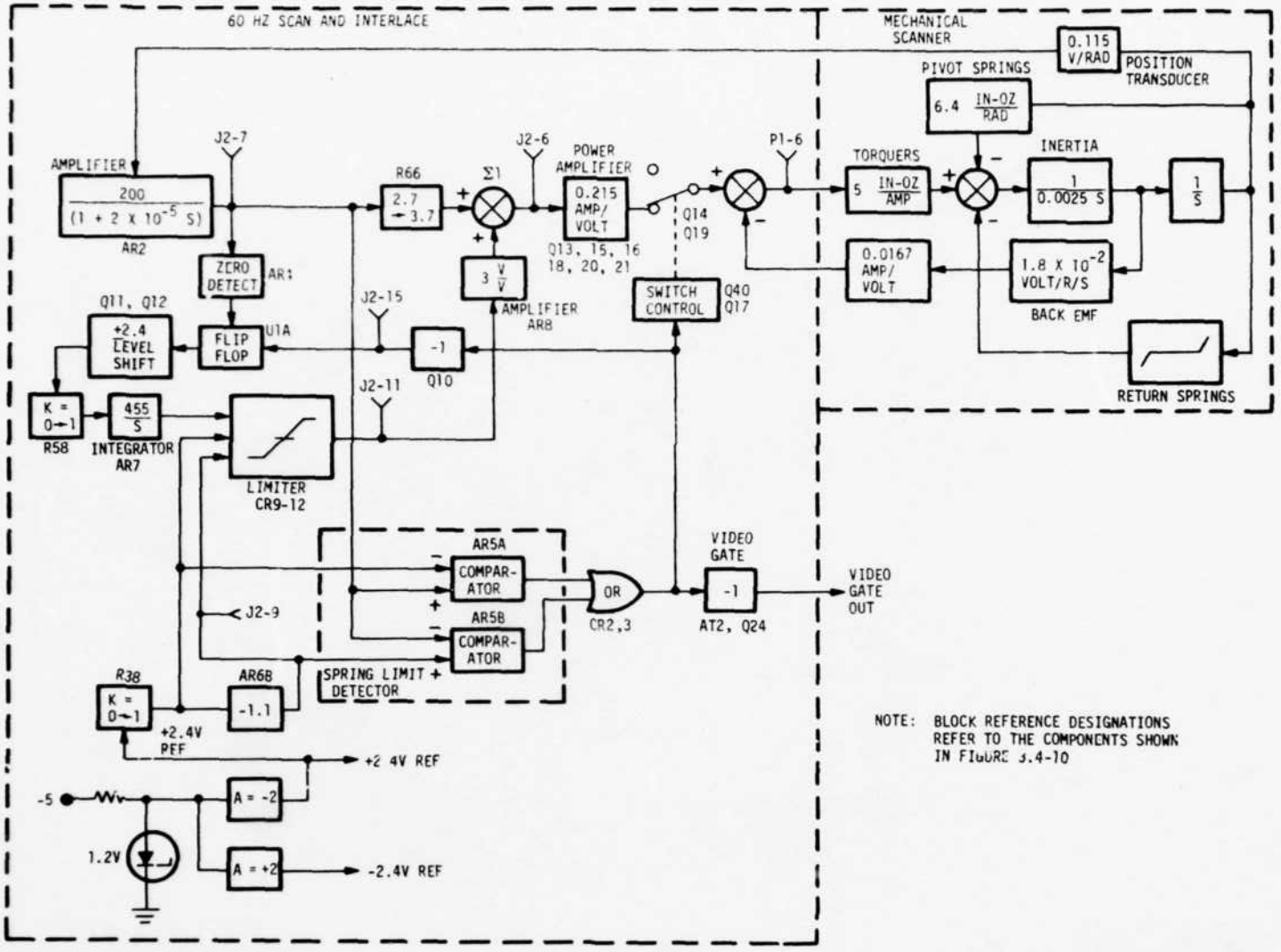


Figure 3.4-11. Scan Position Control Loop

3.4.1.2 Video Electronics Bandwidth

There are many contributors to the overall bandwidth of the complete video chain from the detector to the LED. This bandwidth must be known to predict unique system requirements as well as for noise analysis and for the determination of the phase shift at a given frequency (required to design the phase shift lens described in paragraph 3.4.1.3).

Figure 3.4-12 shows the contributors to the overall system bandwidth. The detector photo conversion time constant is approximately 1 μs which is represented by the $R_D C_D$ time constant. The other resistors and capacitors have the values described in the module schematics (Figure 3.4-13).

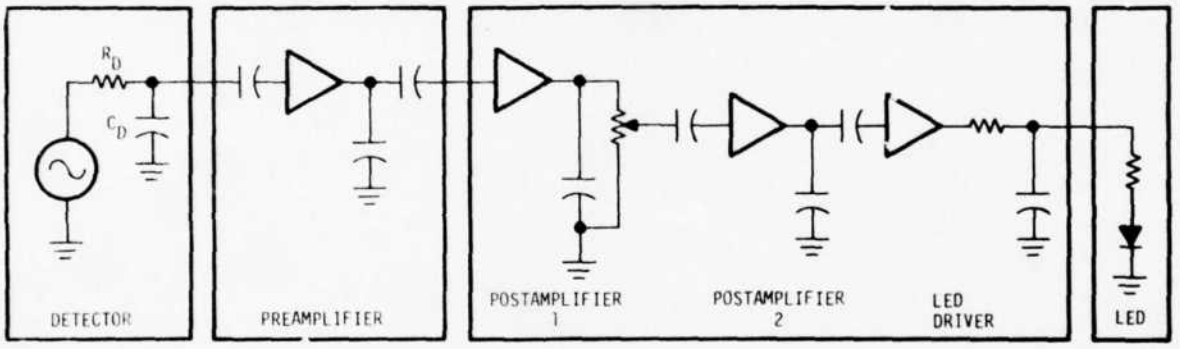


Figure 3.4-12. System Bandwidth Equivalent Circuit

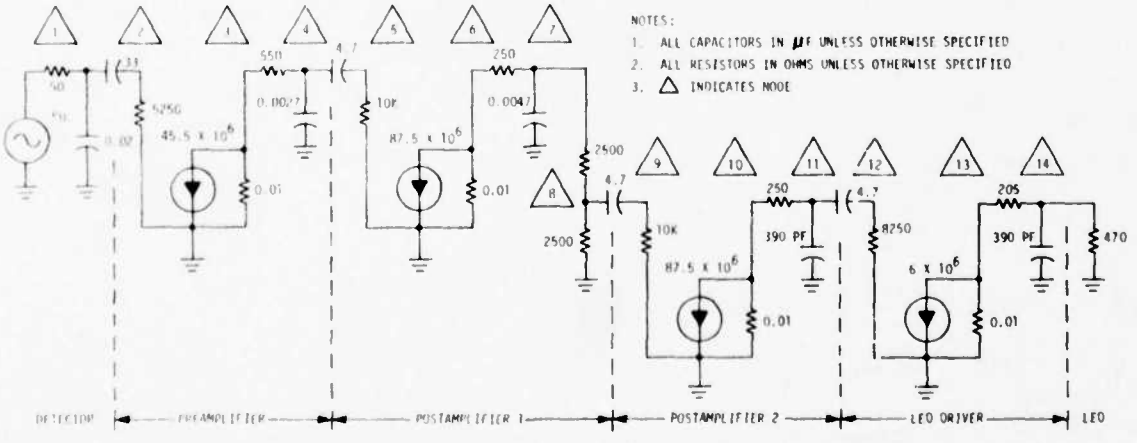


Figure 3.4-13. Video Chain Equivalent Circuit

An equivalent circuit for the overall video chain is shown in Figure 3.4-13, and the ECAP program for this equivalent circuit is shown in Figure 3.4-14. The results of the program yield bandwidths (Figure 3.4-15) in which component values have been adjusted to their absolute worst-case initial values to yield maximum and minimum values as well as the nominal value. The results indicate the following: for the high frequency 3 dB breakpoint, f_{3dB} equals 70 kHz nominal, 80 kHz maximum, and 50 kHz minimum; for the low-frequency breakpoint, f_{3dB} equals 7 Hz nominal, 10.5 Hz maximum, and 4 Hz minimum. For information purposes, the ECAP programs used for the maximum and minimum bandwidths are shown in Figures 3.4-16 and 3.4-17. A thorough discussion of system bandwidth considerations is provided in Appendix B.

```
C       FREQUENCY RESPONSE FOR THE COMPLETE VIDEO CHAIN FROM THE DETECTOR
C       TO THE TED OUTPUT 2/11-76
        AC ANALYSIS
R1      N(0,1),R=50,E=1
R2      N(1,2),C=33E-6
R3      N(2,0),R=5250
R4      N(0,3),R=.01
R5      N(3,4),R=550
R6      N(4,0),C=2200E-12
R7      N(4,5),C=4.7E-6
R8      N(5,0),R=1E4
R9      N(0,6),R=.01
R10     N(6,7),R=250
R11     N(7,0),C=4700E-12
R12     N(7,8),R=2500
R13     N(8,0),R=2500
R14     N(8,9),C=4.7E-6
R15     N(9,0),R=1E4
R16     N(0,10),R=.01
R17     N(10,11),R=250
R18     N(11,0),C=390E-12
R19     N(11,12),C=6.24E-6
R20     N(12,0),R=8250
R21     N(0,13),R=.01
R22     N(13,14),R=205
R23     N(14,0),C=390E-12
R24     N(14,0),R=470
R25     N(1,0),C=2E-8
T1      B(3,4),BETA=45.5E6
T2      B(8,9),BETA=87.5E6
T3      B(15,16),BETA=87.5E6
T4      B(20,21),BETA=6E6
        FREQUENCY=1E3
        PRINT,VOLTAGES
        EXECUTE
```

Figure 3.4-14. Video Chain Bandwidth Program

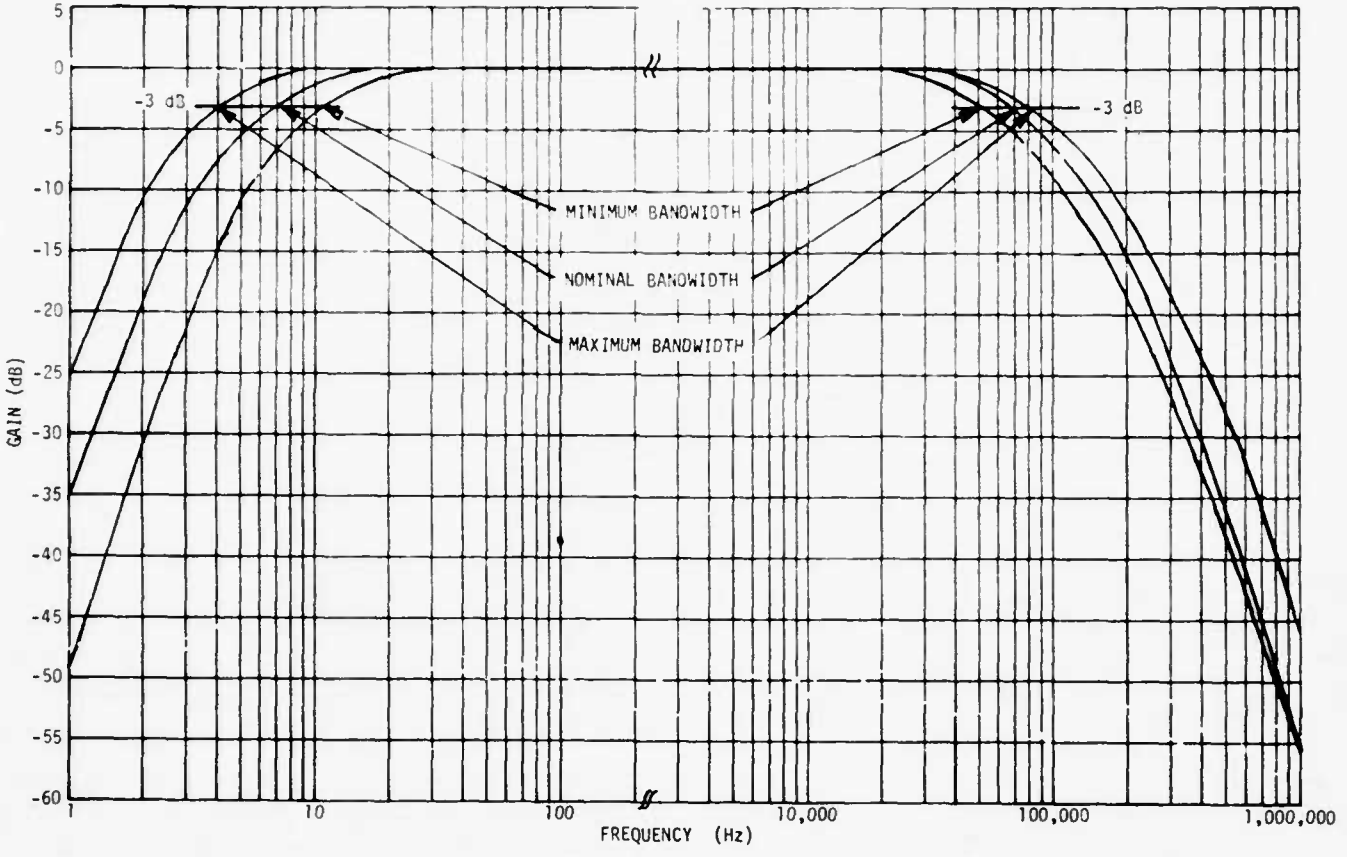


Figure 3.4-15. Video Electronics Bandwidths

```
00010 C     VIDEO CHAIN FROM DETECTOR TO LED FREQUENCY ANALYSIS FOR MAX.BW.
00020 C     ALL COMPONENT VALUES ARE AT THE WORST CASE INITIAL TOLERANCE
00025 C     THIS INCLUDES THE EEEECTS OE THE DETECTOR TIME CONSTANT LINE 305
00026 C     ALSO CHANGES THE MIDRANGE GAIN ...2/13/76
00030 C     CONDITION TO YEILD MAXIMUM BW.
00040 C     INPUT AT NODE 1 (DETECTOR OUTPUT),OUTPUT AT NODE 14 (LED ASSY.).
00050 C     TEMPERATURE AT 25 DEGREES C.   7-30-75
00060       AC ANALYSIS
00070 R1    N(0,1),R=50,E=1
00080 R2    N(1,2),C=39.6E-6
00090 R3    N(2,0),R=6500
00100 R4    N(0,3),R=.01
00110 R5    N(3,4),R=400
00120 R6    N(4,0),C=2430E-12
00130 R7    N(4,5),C=5.64E-6
00140 R8    N(5,0),R=12500
00150 R9    N(0,6),R=.01
00160 R10   N(6,7),R=100
00170 R11   N(7,0),C=4230E-12
00180 R12   N(7,8),R=2625
00190 R13   N(8,0),R=2625
00200 R14   N(8,9),C=5.64E-6
00210 R15   N(9,0),R=12500
00220 R16   N(0,10),R=.01
00230 R17   N(10,11),R=100
00240 R18   N(11,0),C=351E-12
00250 R19   N(11,12),C=5.64E-6
00260 R20   N(12,0),R=10000
00270 R21   N(0,13),R=.01
00280 R22   N(13,14),R=203
00290 R23   N(14,0),C=351E-12
00300 R24   N(14,0),R=470
00305 R25   N(1 0),C=3E-8
00310 T1    B(3,4),BETA=45.5E6
00320 T2    B(8,9),BETA=87.5E6
00330 T3    B(15,16),BETA=87.5E6
00340 T4    B(20,21),BETA=6E6
00350       FREQUENCY=1E3
00360       PRINT,VOLTAGES
00370       EXECUTE
00380       MODIFY
00390       FREQUENCY=1(2)1E6
00400       EXECUTE
00410       END
```

Figure 3.4-16. ECAP Maximum Bandwidth Program

```
00010 C     VIDEO CHAIN FROM DETECTOR TO LED FREQUENCY ANALYSIS FOR MIN.BW.
00020 C     ALL COMPONENT VALUES ARE AT THE WORST CASE INITIAL TOLERANCE
00025 C     THIS INCLUDES THE EFFECTS OF THE DETECTOR TIME CONSTANT LINE 305
00026 C     ALSO CHANGES THE MIDRANGE GAIN ...2/13/76
00030 C     CONDITION TO YEILD MINIMUN BW.
00040 C     INPUT AT NODE 1 (DETECTOR OUTPUT),OUTPUT AT NODE 14 (LED ASSY.).
00050 C     TEMPERATURE AT 25 DEGREES C.   7-30-75
00060       AC ANALYSIS
00070 R1    N(0,1),R=50,E=1
00080 R2    N(1,2),C=26.4E-6
00090 R3    N(2,0),R=4000
00100 R4    N(0,3),R=.01
00110 R5    N(3,4),R=700
00120 R6    N(4,0),C=2970E-12
00130 R7    N(4,5),C=3.76E-6
00140 R8    N(5,0),R=7500
00150 R9    N(0,6),R=.01
00160 R10   N(6,7),R=400
00170 R11   N(7,0),C=5170E-12
00180 R12   N(7,8),R=2625
00190 R13   N(8,0),R=2625
00200 R14   N(8,9),C=3.76E-6
00210 R15   N(9,0),R=7500
00220 R16   N(0,10),R=.01
00230 R17   N(10,11),R=400
00240 R18   N(11,0),C=429E-12
00250 R19   N(11,12),C=3.76E-6
00260 R20   N(12,0),R=6500
00270 R21   N(0,13),R=.01
00280 R22   N(13,14),R=207
00290 R23   N(14,0),C=429E-12
00300 R24   N(14,0),R=470
00305 R25   N(1,0),C=1E-8
00310 T1    B(3,4),BETA=45.5E6
00320 T2    B(8,9),BETA=87.5E6
00330 T3    B(15,16),BETA=87.5E6
00340 T4    B(20,21),BETA=3.9E6
00350       FREQUENCY=1E3
00360       PRINT,VOLTAGES
00370       EXECUTE
00380       MODIFY
00390       FREQUENCY=1(2)1E6
00400       EXECUTE
00410       END
```

Figure 3.4-17. ECAP Minimum Bandwidth Program

The nominal voltage gain of the system is approximately 2.69×10^6 V/V or 129 dB with the ac gain potentiometer set at near maximum and the gain commands 1 and 2 providing minimum attenuation. The gain commands allow for a minimum gain control range of 30 dB (contrast), while the ac gain potentiometers in each channel allow for initial gain balance at room temperature.

3.4.1.3 Phase Shift Calculations

Using the computer runs described in paragraph 3.4.1.2, the phase shift contributed by the electronics can be calculated directly from the computer runs for various sinusoidal frequencies because the printout provides phase as well as amplitude information. If the phase, γ, is given at a particular frequency, f, the delay, Δt, can be calculated using the follow-following equation:

$$\Delta t = \frac{\gamma}{f} \cdot \frac{1}{360°} = \tau \text{ seconds.}$$

The results of this expression for various frequencies for nominal, maximum, and minimum bandwidth conditions are shown in Table 3.4-III. These data indicate that the phase shift lens should be designed for a nominal delay of 3.6 μs for all bandwidths of interest up to 100 kHz.

3.4.1.4 Inverter Electronics

The inverter module supplies a universal drive motor located within the cooler module with two-phase, 115 Vac, 400 Hz power when this power is not already available. Prime power into this unit is 24 $\pm$4 Vdc. Additional circuits within the module provide overload protection. Circuit schematics are provided in Appendix A.7.

TABLE 3.4-III

Phase Shift for Various Frequency and Bandwidth Conditions

Frequency, f (kHz)	Bandwidth Condition	Phase, γ (degrees)	Phase Shift, Δt (μs)
131.1	Nominal	138.02	2.93
65.5	Nominal	80.45	3.41
32.8	Nominal	42.35	3.59
16.38	Nominal	21.45	3.64
8.19	Nominal	10.71	3.63
4.10			
131.1	Minimum	111.42	2.36
65.5	Minimum	47.51	2.73
32.8	Minimum	33.87	2.87
16.38	Minimum	17.16	2.91
8.19	Minimum	8.57	2.91
131.1	Maximum	147.50	3.13
65.5	Maximum	92.86	3.93
32.8	Maximum	51.17	4.33
16.38	Maximum	26.32	4.46
8.19	Maximum	13.17	4.47

3.4.2 System Interconnects

3.4.2.1 Video Electronics Interconnects

Only the interconnection of the video electronics modules will be considered in this section. The interconnects to the inverter, scan and interlace, and scanner module are rather straightforward and are described in sufficient detail in paragraph 3.4.1 or in Appendix A.

A typical hookup for an 80-channel system is shown in Figure 3.4-18. Typically, the interconnects between the detector module and preamplifier module are flex harnesses, as are the interconnects between the preamplifier module and the postamplifier/control driver module (top of the printed circuit boards) and between the postamplifier/control driver and LED array modules. For production applications, it is assumed that

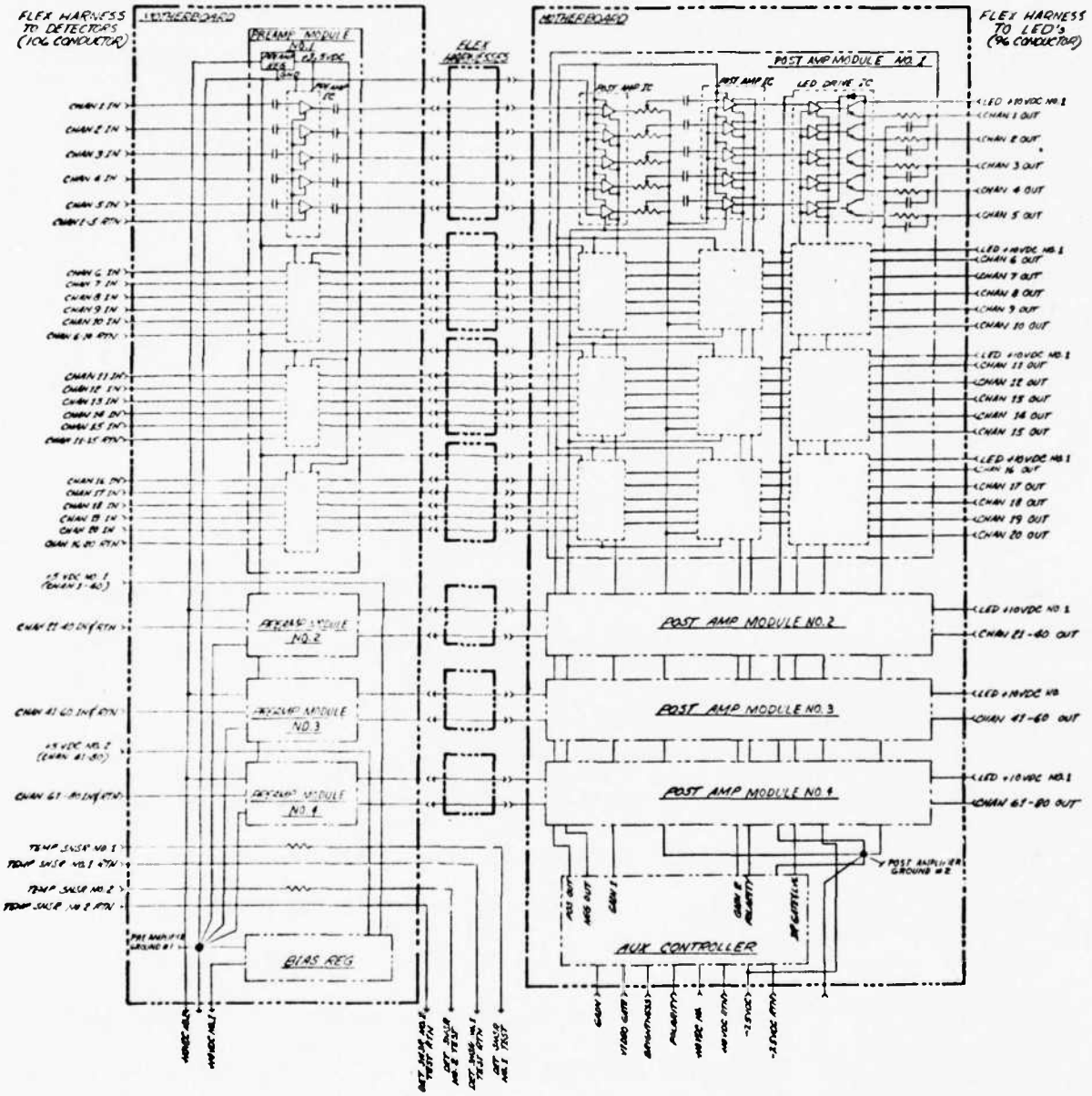


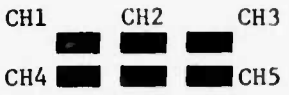
Figure 3.4-18. Video Electronics Typical Interconnection Diagram

printed circuit board interconnects are made via motherboard. The preamplifier, bias regulator, postamplifier/control driver, and auxiliary control modules should be located on a single motherboard. If one motherboard is not possible due to physical constraints of the system, then the logical division should be one motherboard to handle the preamplifier and bias regulator modules and another to handle the auxiliary control and postamplifier/control driver modules.

There are four preamplifier ICs per module with a density of five channels per IC thus providing 20 channels per module. Each postamplifier/control driver module contains 20 channels with two postamplifiers in series cascaded with a third LED driver IC to form one channel out of the 20. To reiterate, there are 20 channels for each preamplifier module grouped in quantities of five channels (per IC), and there are 20 channels for each postamplifier/control driver module grouped in quantities of five channels (per IC).

3.4.2.2 Video Electronics Physical Considerations

Experience in the use of low-level signal systems has demonstrated the criticality of shielding to prevent EMI from disturbing system performance. It can be shown that the minimum signal levels between the detector and preamplifier are as low as 2 or 3 μV. This dictates the need for short distances between the detector output and the preamplifier input. Similarly it requires grouping of the wires from the detectors equally spaced about the return. This produces common-mode pickup equally on the six lines and at the input to the preamplifier, and consequently adds to a desired input of zero volts differentially. For flex harnesses, a typical two layer pattern for the channels might appear as:



Furthermore, the use of a shielded cable between the detector and the preamplifier may be required.

Further investigation demonstrates the need for an EMI-shielded enclosure around the video electronics, or as a minimum, a complete metal enclosure. This protects the module circuitry as well as the flex interconnects between the preamplifier module and postamplifier/control driver module. The signal levels between the preamplifier and postamplifier are at least an order of magnitude less sensitive to EMI than the interface between the detectors and the preamplifier. The LED driver and LED interface is the least sensitive compared to other areas and no special precautions are warranted.

Most of the interface descriptions so far have dealt primarily with systems that have external EMI-induced noise. Systems containing only self-induced EMI have been developed which operate rather well with no shielding between the preamplifier and detector (6 inches in length) and no EMI enclosure for the electronics. In these systems, the only internal source of EMI was that of the scanner (30 Hz) and the power supply dc/dc converter (which was shielded with metal). There was no image intensifier or mechanical cooler used, the latter function being performed by an open-cycle Joule-Thompson cooler system.

3.4.2.3 Video Electronics Grounding

The grounding of the video electronics is of primary importance because these circuits are the most susceptible to line-conducted and radiated sources of noise. The grounding of the scanner and cooler is covered in the next section.

The design of the modules has limited the user to one basic grounding technique which is believed to be an acceptable one within the constraints of good design practices. The video electronics interconnect diagram is shown in Figure 3.4-18 for a typical 80-channel system.

The grounds of the preamplifier modules and the bias regulator module are returned to one common tie-point, which is the preamplifier ground 1, as shown in Figure 3.4-18. (This is true even if only one motherboard is used.) This ground is taken to the power supply star ground which is the video electronics holy point. Similarly, the postamplifier/control driver module grounds and the ground of the auxiliary control module are tied to the postamplifier ground 2. This in turn is taken to the power supply star ground. Finally, the LED high-current returns are brought back to the power supply ground. In many system applications, the LED returns may be routed through the motherboard.

An expanded version of the video electronics connections is shown in Figure 3.4-19 for one channel. Ground integrity is maintained between the detectors and preamplifiers by bringing the return of the detector to the preamplifier ground input. Ground integrity is maintained between the preamplifier and postamplifier because the postamplifier 1 has high common mode rejection and both inputs are referenced back to the preamplifier ground. The output stage of the first postamplifier is referenced to the postamplifier 2 ground as are the second postamplifier and the LED driver.

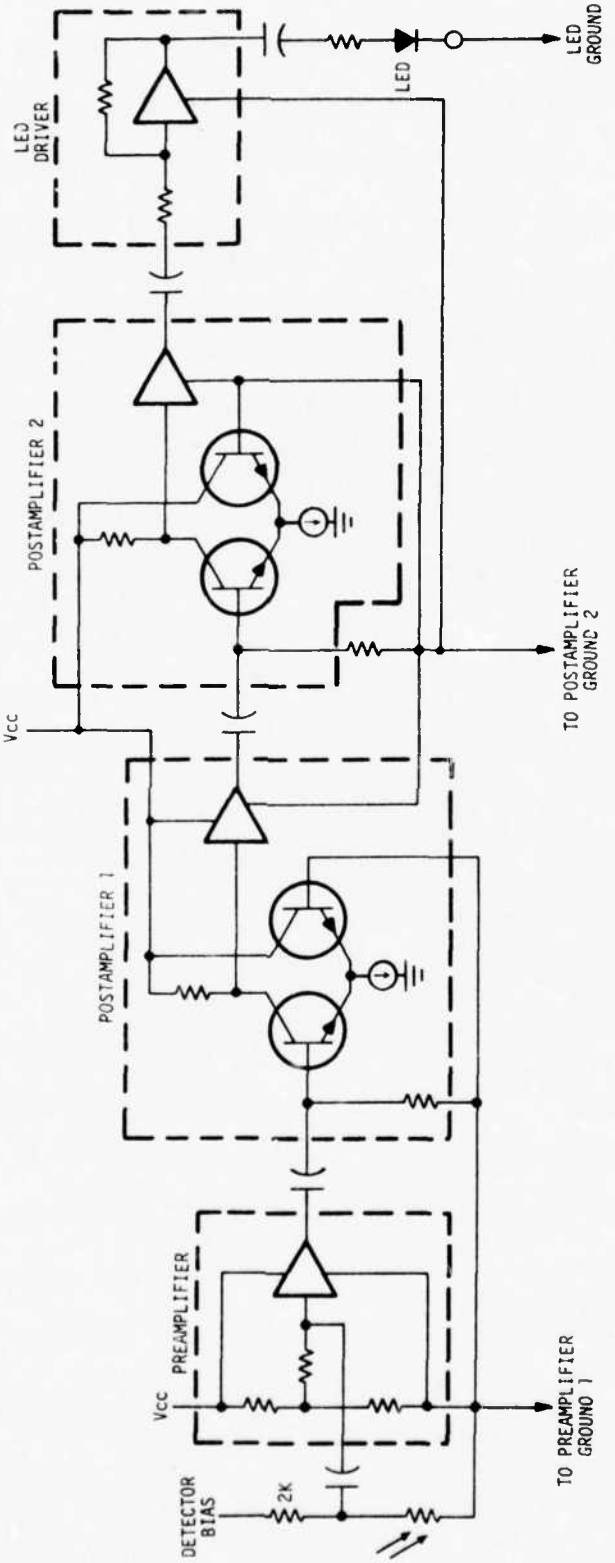


Figure 3.4-19. Video Electronics Connections for One Channel

3.4.2.4 High-Power System Interconnect

For information purposes, a system interconnect diagram is shown in Figure 3.4-20 for a system containing the following: 80 channels, I^2T, Stirling cycle cooler, and 60 Hz scanner. Special attention is addressed to the following features:

1 The power (+24 Vdc No. 2) to the inverter module is shielded, and is carried separately all the way back to prime power to reduce line-conducted interference.

2 Image intensifier power leads are twisted to reduce EMI.

3 Focus control is motor driven with limit switches.

4 A system circuit breaker and test point connector are provided.

5 The interface for the transducers between the mechanical scanner module and the scan and interlace module are shielded to reduce the effects of external EMI. The signal levels on these interconnects are in the millivolt range.

3.4.3 Power Supply Considerations

3.4.3.1 High-Power Mode

The HP mode refers to the mode of operation in which the prime source is not run-time limited, i.e., efficiency is an important requirement but run time is not reduced by the amount of power consumed (such as with a battery prime source). For most HP mode applications, all the common modules are used (including the Stirling cycle cooler).

To best describe the HP mode of operation, an example of an HP system is given. Assume the following requirements:

1 Prime power: 24 $\pm$ 4 Vdc

2 Power supply efficiency: 70 percent minimum

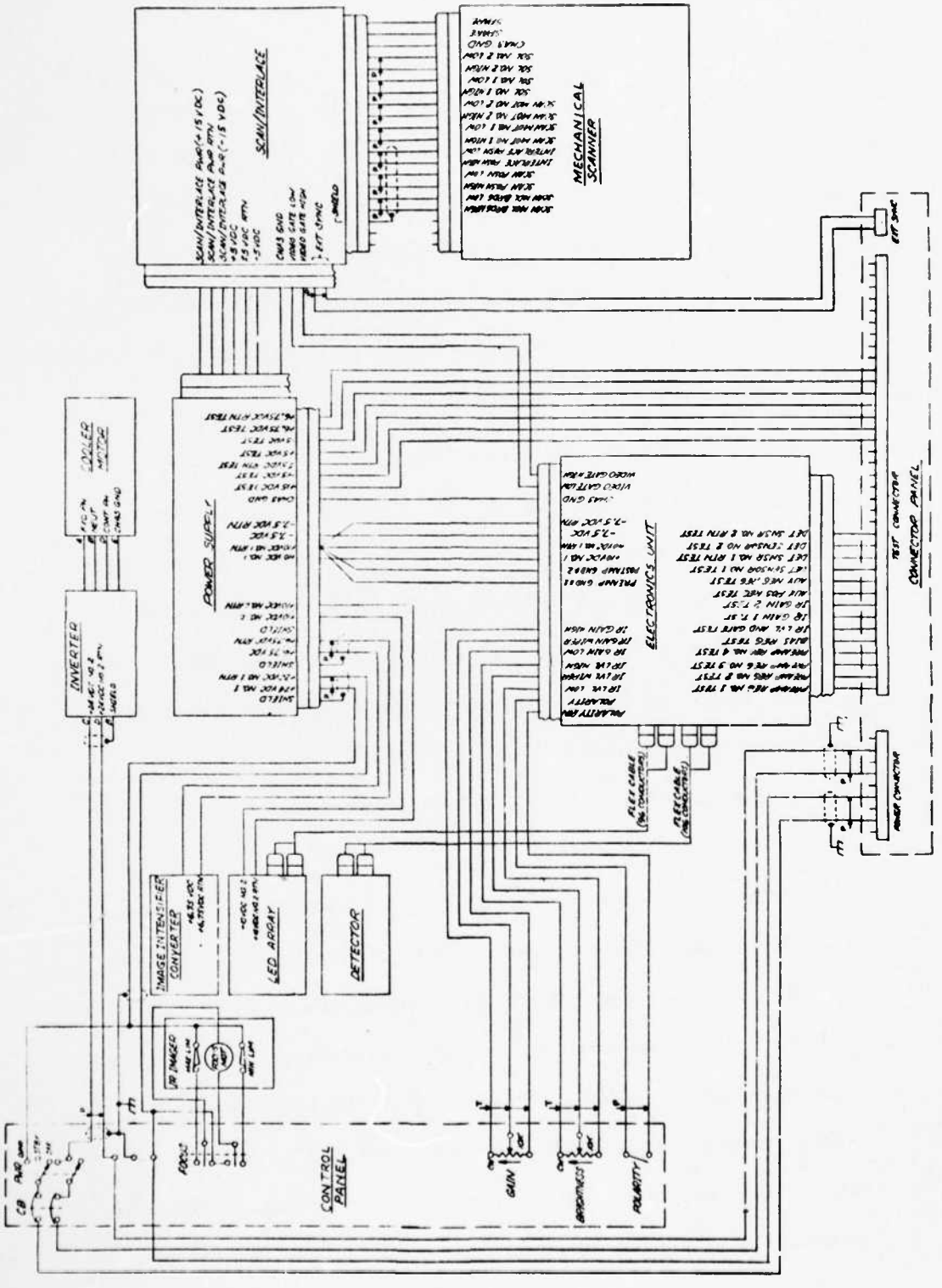


Figure 3.4-20. Typical 80-Channel System Interconnection

3 System channel capacity: 180 channels

4 Scanner speed: 60 Hz

5 Cooler type: Stirling cycle (closed cycle, mechanical)

6 Additional requirements: Image intensifier tube to be used

7 Special features: Overvoltage protection
Input voltage reversed protection
Power supply turn-on sequence (required by the scan and interlace module B2 specification).

With these requirements, the following sequence is followed to arrive at an acceptable design for the 180-channel system.

1 The inverter power for the cooler is derived from prime +24 Vdc input and will not be considered in the power supply design. The input power to the inverter is approximately 65 watts.

2 An efficiency of 70 percent is a mandatory minimum specification.

3 Due to the efficiency and input voltage range requirements, a switching preregulator will be required.

4 Due to the negative voltages and efficiency requirements, a converter will be required.

5 The converter frequency is 20 kHz. It is predicated on past experience that this frequency yields the best compromise of the size, weight, and efficiency requirements.

6 Because of the low-noise and low-EMI environment, special precautions will be taken in the design of the converter to minimize common mode switching transients and noise. In particular, the converter will be a non-self-oscillating, non-saturating type with built-in dead zones during the times of

switching. This requires an internal oscillator that supplies the driver transistors of the converter.

7 Because of common-mode coupling between the primary of the converter and the secondary, Ballentine transformers will be used to isolate the common mode transients on the critical voltages (+10 Vdc No. 1 and +10 Vdc No. 2; -7.5 Vdc), and these voltages will be isolated from the other windings of the transformer by a Faraday shield. Also, the video electronics return will be isolated from all other returns via the converter transformer.

8 The switching preregulator will be synchronized to the converter.

9 For ease of implementation, the following voltages will be selected to represent what is believed to be the minimum number required within the constraints of good design practice. A tolerance of ±5 percent is adequate for all requirements.

+10 Vdc No. 1 - For the bias regulator, preamplifier, and auxiliary control modules (more filtering required than for +10 Vdc No. 2)

+10 Vdc No. 2 - LED supply on the postamplifier/control driver module (less filtering required than for the +10 Vdc No. 1)

-7.5 Vdc - For the auxiliary control and postamplifier/control driver modules (LED driver)

+5.0 Vdc - Scan and interlace

-5.0 Vdc - Scan and interlace

+15.0 Vdc - Scanner motor and solenoid drive

-15.0 Vdc - Scanner motor and solenoid drive

-6.75 Vdc - Image intensifier tube supply

If a 30 Hz scan rate is used, the scanner motor and solenoid can be driven from the ±5 Vdc supplies and the ±15 Vdc will not be required.

10 The current requirements (Figure 3.4-21) will be determined for each voltage.

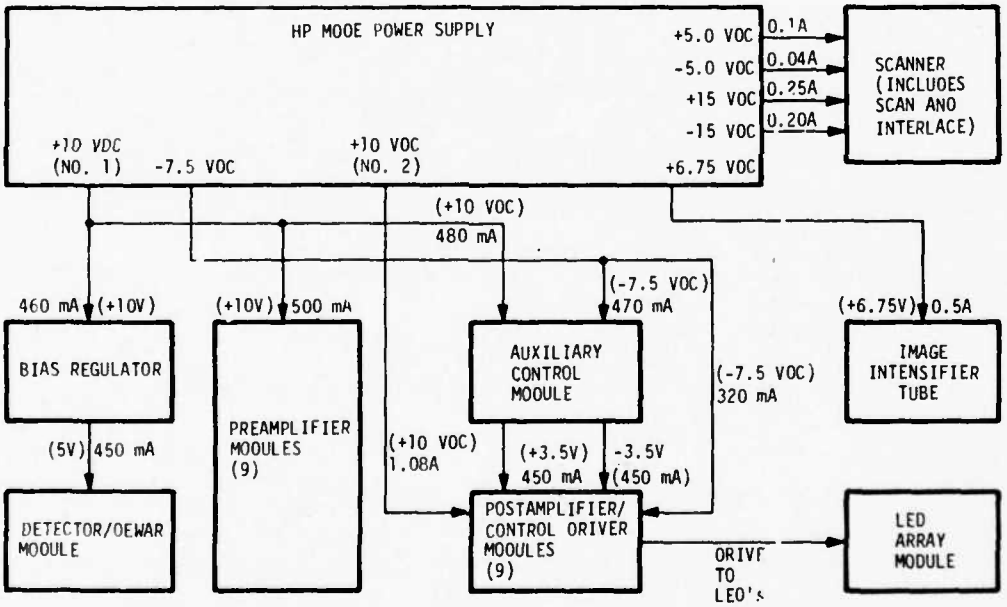


Figure 3.4-21. Current Requirements

a +10 Vdc No. 1 - Total current is 1.41 amperes. The average current for each detector element with +5 Vdc bias out of the bias regulator as described in Appendix A.1 is 2.5 mA per detector. Therefore, the average current required by the detectors is 2.5 mA times 180 or 450 mA. The bias regulator itself requires about 12 mA as determined by analysis. The total current required by the bias regulator from +10 Vdc No. 1 is 460 mA, of which 450 mA is delivered to the detector array on the 5 Vdc line. Each preamplifier module requires 55 mA, making a total of approximately 500 mA for nine modules. The auxiliary control module supplies current to all postamplifiers on the postamplifier/control driver modules. This is specified to be 28 mA plus 2.5 mA per channel, which equals approximately 480 mA. The 2.5 mA per channel is delivered to the postamplifier/control driver module via the +3.5 Vdc interconnect (450 mA).

b +10 Vdc No. 2 - Total current is 1.08 amperes. The requirement for the nominal current to the LEDs has been determined by analysis to be in the range of 4 mA. For a 180-element array, the total current becomes 180 times 4 mA or 720 mA. The LED drivers also require current on the module at 10 mA per IC which is 40 mA per module or 360 mA for nine modules.

c -7.5 Vdc - Total current is 0.79 ampere. The requirement for the auxiliary control module (which supplies the postamplifier/control driver module via the -3.5V interconnect) is specified to be 21 mA plus 2.5 mA per channel or 470 mA. The requirement for the postamplifier/control driver module is specified to be 35 mA per module times nine modules or 320 mA.

d +6.75 Vdc - Total current is 0.5 ampere. The input current to the image intensifier tube is specified to be 0.5 ampere.

e Scanner Power(+5.0, -5.0, +15.0, and -15.0 Vdc) - Total power is approximately 7.5 watts. The scanner can be operated with only +5.0 and -5.0 Vdc if rates of less than 30 Hz are maintained. This system is specified to operate at 60 Hz, which requires the use of both the +15.0 and -15.0 Vdc supplies in addition to the +5.0 and -5.0 Vdc supplies. The total power specified for the scanner electronics is 7.5 watts in the 60 Hz mode and 4.0 watts in the 30 Hz mode. Table 3.4-IV summarizes the current and power that were determined from analysis for this system.

TABLE 3.4-IV

Scanner Current and Power Requirements

Input (Vdc)	Current (amperes)	Power(watts)
+15.0	0.25	3.75
-15.0	0.20	3.0
+5.0	0.10	0.5
-5.0	0.04	0.2

11 Ripple and Transient Requirements. The fundamental converter frequency ripple of 20 kHz is the most easily predicted and accounted-for ripple in the design cycle. The difficult requirement is suppression of the high frequency switching transients of the converter and switching preregulator, both line-conducted and radiated. Line-conducted transients are best suppressed by the use of Faraday shields, Ballentine transformers, and conventional filtering. The radiated EMI is best controlled by

proper EMI shielding of the complete power supply, with the use of a complete metal enclosure as a minimum. Past experience with FLIR systems has demonstrated the need for radio frequency interference shielding for all switching-type regulators and converters, and this includes the image intensifier tube. The reduction of EMI by the use of slower switching speeds in the converter can drastically reduce efficiency, and shielding is the preferred method of control. Table 3.4-V shows ripple requirements determined as a result of analysis or by the B2 specification for the module.

TABLE 3.4-V

Ripple Requirements

Voltage (dc)	Ripple (mVrms)	Determined by
+10 (No.1)	1	Analysis
+10 (No.2)	100	Specification
-7.5	35	Analysis
+6.75	50	Specification
+5.0	35	Specification
-5.0	35	Specification
+15.0	70	Specification
-15.0	70	Specification

12 A major consideration is that there should be a turn-on sequence for the voltage supplied to the scanner electronics. The +15 Vdc and -15 Vdc turn-on rise time will be equal to or less than that of the +5 Vdc and -5 Vdc supplies.

13 Table 3.4-VI summarizes the HP mode power supply requirements.

TABLE 3.4-VI

High-Power Mode Power Supply Requirements

Voltage (dc)	Tolerance (%)	Current (A)	Ripple (mVrms)	Power (W)
+10.0 No. 1	±5	1.41	1	14.10
+10.0 No. 2	±5	1.08	100	10.80
-7.5	±5	0.79	35	5.93
+6.75	±5	0.50	50	3.38
+5.0	±5	0.10	35	0.50
-5.0	±5	0.04	35	0.20
+15.0	±5	0.25	70	3.75
-15.0	±5	0.20	70	3.00
				41.66
Power Supply Power $41.66 \cdot \frac{1}{0.70} - 41.66$				17.85
Cooler Power				65.00
Total System Power				124.51

3.4.3.2 Low-Power Mode

The LP mode will be considered to be a battery-operated system such as might be used in a man-portable system. For this type of system, the need for LP is a necessity to increase minimum run time. Usually, the number of channels is reduced and voltages are decreased to provide for a lower power consumption by the system. Also, in these LP systems a Joule-Thompson (open-cycle, air-cooled) cooler is normally used, which requires no electrical power and has a normal minimum run time of 2 hours. The scanner consumes less power at slower speeds and will be assumed to be 30 Hz.

To best describe the differences between the HP and the LP modes, the deviations from the HP procedure are listed below.

1 Scanner - The 60 Hz scanner can be run at a 30 Hz rate with a maximum power consumption of 4.0 watts. For the 30 Hz rate, the scanner can operate from only +5.0 and -5.0 Vdc supplies with the +15.0 Vdc and -15.0 Vdc supplies not required. Now the scanner requirements become:

Voltage(dc)	Tolerance(%)	Current(A)	Ripple(mVrms)	Power(W)
+5.0	±5	0.47	35	2.35
-5.0	±5	0.33	35	1.65

2 The auxiliary control can have lower voltages on the pass stages of the module. In particular, the module input pins 23 and 25 can have +5.0 Vdc and -5.0 Vdc, respectively. Pins 18 and 20 will still require +10 and -7.5 Vdc, respectively. Note that the output of the regulators on pins 3 and 21 will be limited to +3.50 Vdc and -3.50 Vdc maximum in LP operation. The LP requirements for the auxiliary control are: (60 channels)

Voltage(Vdc)	Tolerance (%)	Current(A)	Ripple(mV)	Power(W)
+10	±5	0.028	35	0.28
+5	±5	0.075	35	0.38
-5.0	±5	0.075	35	0.38
-7.5	±5	0.021	35	0.15

3 The postamplifiers of the postamplifier/control driver module are supplied by the auxiliary control module power while the LED drivers are supplied by the power supply. In the LP mode, the LED supply will be 5.0 Vdc (pin 32 of the module), while the negative supply to

the LED drive will be -5.0 Vdc. The current requirement per module now becomes:

Voltage (Vdc)	Current (mA average)
+5.0	90
-5.0	30
+10.0	30

This estimate does not include the +3.5 Vdc and -3.5 Vdc currents accounted for in the auxiliary control budget.

3.4.4 Electronic Setup and Alignment Procedures

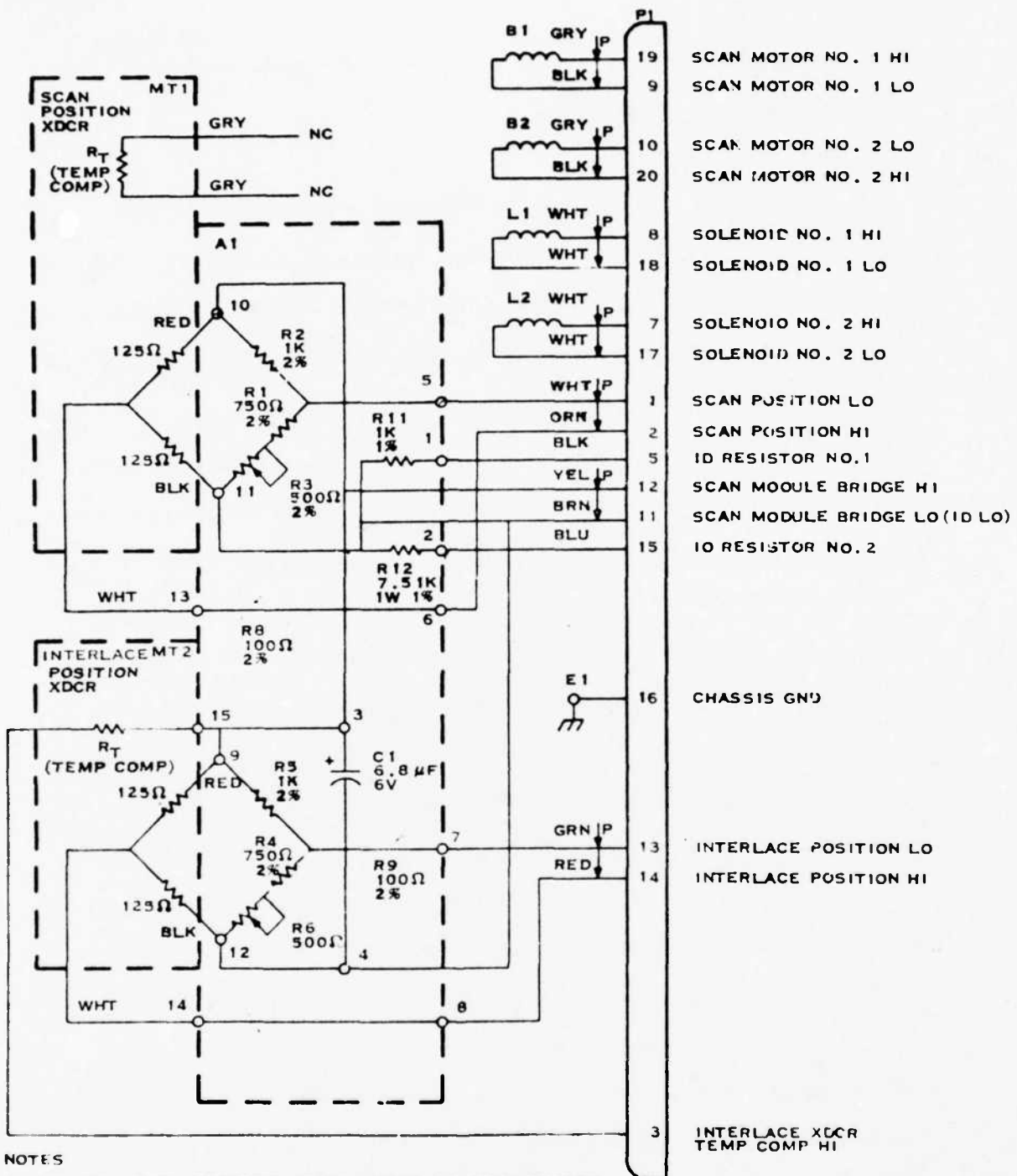
Special setup and alignment procedures are recommended for the mechanical scan and scan and interlace modules and for the video electronics. Electrical interface between the remaining assemblies requires no special procedure.

3.4.4.1 Mechanical Scanner and Scan and Interlace

The scan and interlace module will interface directly with the mechanical scanner. Figure 3.4-22 shows the circuitry associated with the mechanical scanner. As indicated in the figure, there are two torque motors, two solenoids, and two bridge circuits with transducers (Hall-effect devices).

There are two sets of return springs that may be used with the mechanical scanner - 30 Hz and 60 Hz. The 30 Hz springs are quieter but might result in less scan efficiency than the 60 Hz springs.

The following adjustments for the scan and interlace module will require shop facilities:



NOTES

1. MT1 POLARITY–POSITIVE GOING SIGNAL AS SCAN MIRROR IS MOVED CCW (VIEWED FROM SOLENOID END OF SCANNER)
2. MT2 POLARITY–POSITIVE GOING SIGNAL AS THE GIMBAL IS ROTATED CW (VIEWED FROM SOLENOID END OF SCANNER DOWN THE INTERLACE GIMBAL AXIS)
3. MOTOR POLARITY–ROTOR SHOULD MOVE CCW (VIEW FROM LEAD SIDE OF MOTOR) WHEN A POSITIVE CURRENT IS FLOWING IN THE GRAY WIRE.
4. NO. 1 SOLENOID AND MOTOR ARE THOSE CLOSEST TO THE MOODULE CONNECTOR
5. ALL FIXED RESISTORS ARE 1/8 WATT

Figure 3.4-22. Scanner Schematic

1 Frequency change including 20 to 30 Hz low power operation

2 Interlace mode change

3 Scan angle change.

Procedures have been developed to aid in the adjustment of scan frequency, scan angle, and interlace mode setting. The need for test equipment dictates the need for shop facilities. A total adjustment time of approximately 30 minutes is required for either alignment.

3.4.4.1.1 Scan Malfunction Circuits

The scan malfunction and scan failure protection circuits are actually three circuits, two of which are located on the scan and interlace common module and one of which is located on the auxiliary control common module.

The circuits previously mentioned provide video blanking, scan malfunction protection, and a scan malfunction indication. The video gate circuit on the scan and interlace common module and a pulse detection circuit on the auxiliary control common module provide video blanking during the interlace period and video blanking when scanner speed is dramatically reduced or stopped. The first feature removes display nonlinearities due to the scan mirror turnaround and mechanical interlace. The second feature prevents damage that would occur in systems having vidicons as a result of intense LED light being concentrated on a single vertical line on the vidicon target. The scan malfunction indication circuit located on the scan and interlace common module provides an output which can be used to indicate when loss of video is due to a scan malfunction.

Scan malfunction indicator circuitry is located on the scan interlace card and is controlled by Q31, Q37, Q38, and associated components. The control signal for this function is the spring limit detector signal located at J2-16. This signal is coupled through C43 into Q31 causing

Q31 to switch on and off. This action causes C46 to charge and discharge between +5 and -5 volts. The rapid charge through Q31 of C46 toward +5 volts and slow discharge through R153 maintains Q37 in an on state and Q38 in an off state. An indicator connected between +5 or +15V and the collector of Q38 would be off. If the spring limit pulses were to discontinue, the ac coupling action of C43 would cause Q31 to turn off allowing C46 to discharge to -5 volts within 500 ms. At this time, Q37 will be off and Q38 will be on causing the indicator to be on. Capacitor C46 serves a second function in this circuit. It allows a 500 to 700 ms delay at turn-on before the scan malfunction indicator can be turned on.

A circuit on the scan and interlace common module composed of Q36, U3, AT2, and associated components produces a blanking pulse that occurs during the scanner turnaround time. The spring limit detector signal is differentiated by C44 and R156 to produce a 250 μs negative-going pulse at the collector of Q36. This pulse occurs on the leading edge of the spring limit detector signal and serves as the trigger for U3. U3 is a type 555 timer connected as a one-shot. Pulsewidth is controlled by R160 and will be adjusted to be approximately equal to and in phase with the spring limit detector pulse.

Scan failure protection is provided by Q16-Q18 and AR5 of the auxiliary control. The IR gate pulse is received by Q16, which switches Q17 and Q18 to produce a negative-going pulse during blanking. This signal drives inverting amplifier AR5 to produce a positive pulse during blanking, which blanks the LED driver. When pulses disappear, C13 discharges and Q17 is turned off to produce a high level at Q18. This again produces a negative signal into AR5, which causes the LED driver to be blanked in the event of scanner failure.

3.4.4.1.2 Scan Angle Adjustment

To adjust the scan angle:

1 Loosen tne four set screws on the bottom of the scanner, which hold the return springs in place.

2 Install the scanner in a fixture to reflect collimated light onto a flat mirror as shown in Figure 3.4-23.

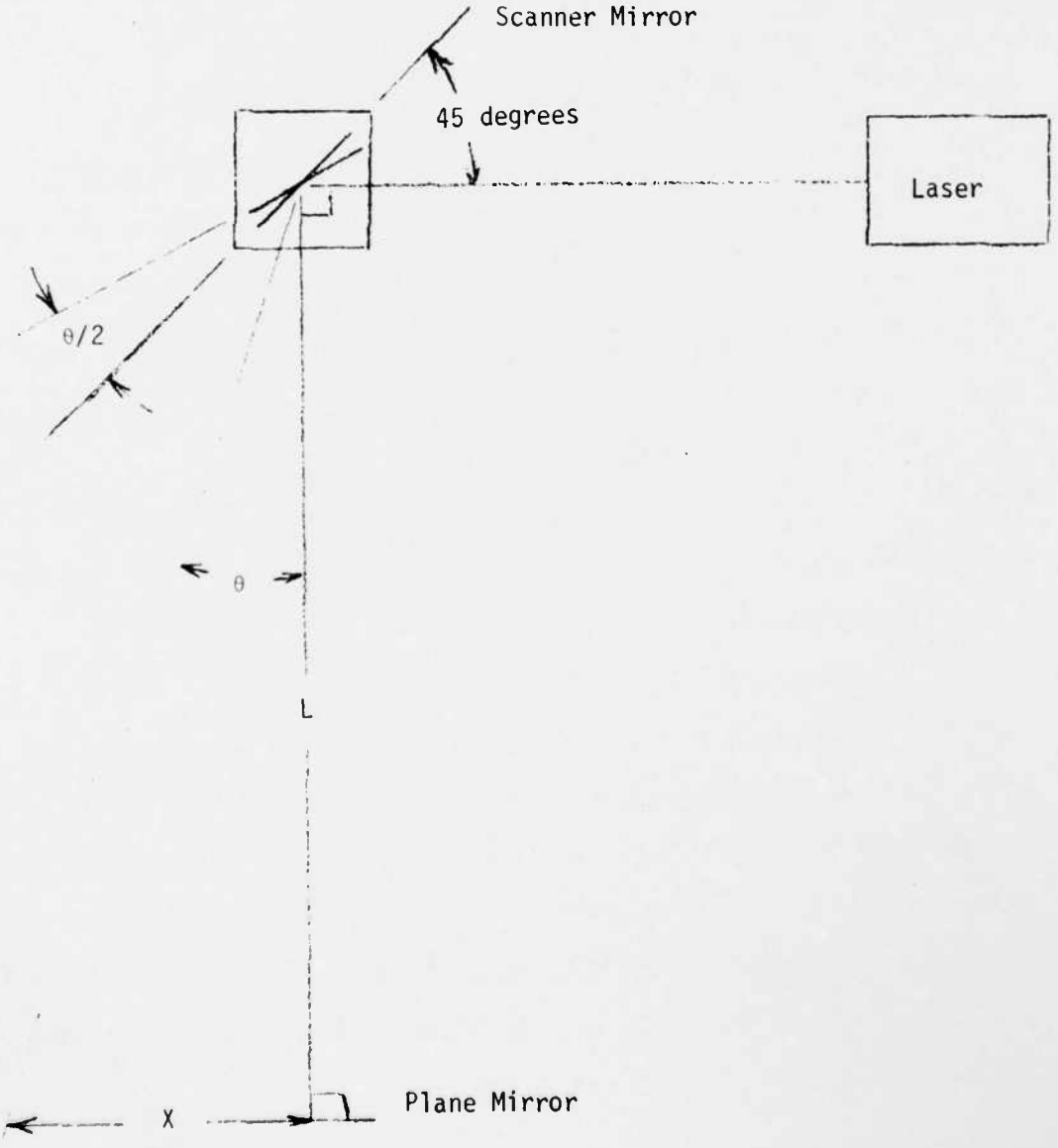


Figure 3.4-23. Scan Angle Setup

3 Manually move the mirror CCW until the return arm just makes contact with the return spring, and adjust one return spring for the proper angle (θ)

$$\theta = 2 \text{ Tan}^{-1} \frac{X}{2L}.$$

4 Manually move the mirror CW and repeat step 3.

5 Using a 0.001 inch shim between the return arm and the return springs, adjust the remaining springs so that contact is made between diagonal front and back springs simultaneously.

6 Verify that the angles measured to steps 3 and 4 have been maintained.

7 Remove the scanner from the fixture, and tighten the return spring setscrews on the bottom of the scanner.

3.4.4.1.3 Scan Transducer Alignment (MT1)

To align the scan transducer:

1 Connect the mechanical scanner and the scan and interlace printed circuit board per Figure 3.4-24.

2 Connect jumpers between +5 Vdc and PI-12 of the PCB to disable the scanner, and between PS-1 (+) and PI-12 of the scanner for manual bridge gain control.

3 Turn power supplies on.

4 Monitor the voltage at PS-1 (+). Adjust PS-1 for 1.9 ± 0.05 Vdc.

5 Remove the scanner side plate to gain access to MT1 target assembly (scan position transducer). Remove MT1 target assembly.

6 With the scan mirror at rest position, adjust R3 (top pot) on the scanner for 0.000 ± 0.005 Vdc.

CAUTION - Do not readjust R3 after this step.

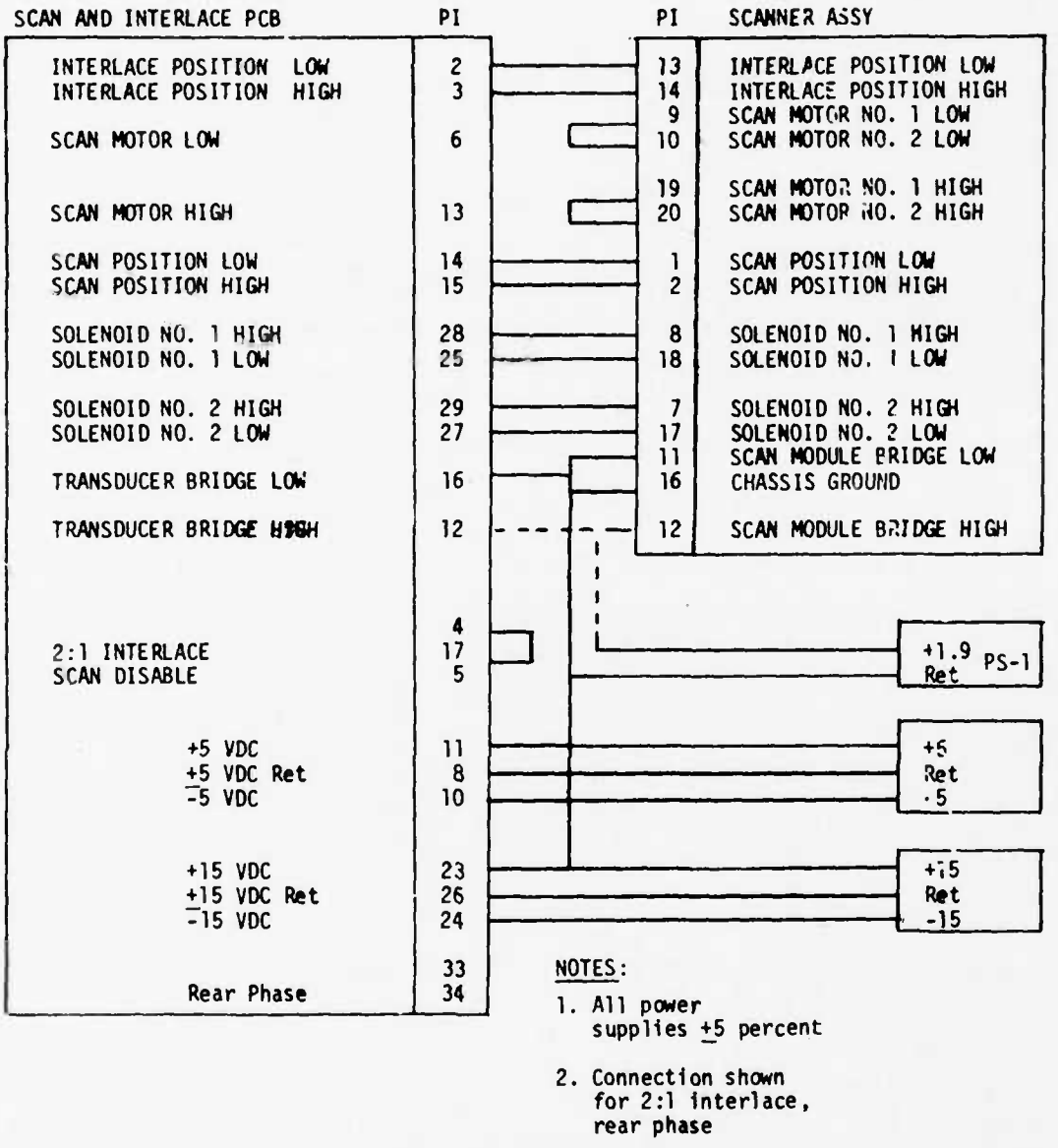


Figure 3.4-24. Scanner Test Interconnect

7 Reinstall MTI target assembly on UUT.

8 Move and hold scan mirror against spring stop CW as viewed from top of scanner. Adjust target assembly vertically (up or down) to achieve an amplitude of 420 MV. Check for the same amplitude CCW of the mirror; adjust

target assembly vertically and MT1 target spacing as required to achieve +420 and -420 MV. Maintain an offset of 0.000 ±0.005 Vdc while performing the above by allowing the scan mirror to come to rest position and adjusting MT1 assembly in azimuth (left or right).

9 Remove jumper between PI-5 and +5 Vdc to enable scanner.

10 Turn power off, then on, to start the scanner. (Cycling of the power or moving the scan mirror manually may be necessary to start the scanner.) Ensure that the scan and interlace card is set up to operate at 60 Hz. Observe J3 with an oscilloscope. The signal observed should be a 1.0 Vpp ±0.02V symmetrical, triangular waveform operating about ground position. If the waveform is not swinging about ground, readjust transducer azimuth/position. If triangular waveform is not 1.0 ±0.02V p-p, turn power off and readjust the distance between the scan position transducer and the target by loosening the MT1 clamp screws and moving the transducer. Turn the scanner on, and again measure the amplitude of the scan position signal. Readjust the transducer azimuth if necessary. The amplitude of the triangular waveform should be 1.0 ±0.02V p-p. If necessary, readjust the transducer again as stated above.

11 Turn power on, and observe the scan position waveform. If it is not symmetrical and measuring 1.0 ±0.02V p-p, readjust from the beginning step.

3.4.4.1.4 Interlace Position Transducer Alignment (MT2)

To align the interlace position transducer:

1 Ensure that the solenoid stop pins located in the center of each solenoid are not restricting the interlace gimbal motion.

2 Place a jumper between PI-5 and +5 Vdc to disable scan and interlace drive amplifiers.

3 Move the scan mirror. Allowing it to oscillate helps the interlace gimbal to find its natural resting position.

4 Turn power on. Remeasure the bridge voltage at PS-1 with the DVM. Check that the voltage is 1.90 ± 0.05 Vdc. If it is not, readjust the supply as necessary.

5 Monitor J6 of scan and interlace card with a DVM. Adjust R6 on the scanner (bottom pot) of the bridge transducer circuit board to read 0.00 ± 0.01 Vdc of the DVM.

6 Move the interlace gimbal 0.001 inch clockwise from its at rest position, and record the positive voltage at J6 of the PCB. Move the interlace gimbal 0.002 inch CCW and record the negative voltage at J6 of the PCB. Check that the voltage differential between the readings is 0.750 ± 0.025V p-p and approximately centered about 0. If it is not, signal amplitude may be changed by varying the spacing between MT2 (interlace position transducer) and its target. Centering may be changed by varying the target position.

CAUTION - All adjustments should be made in the at-rest position while maintaining 0.00 ± 0.01 Vdc at J6 of the PCB by adjusting R6 of the scanner. Repeat steps 5 and 6 as necessary.

3.4.4.1.5 Interlace Motion Stop Pin Adjustment

To adjust the interlace motion stop pin:

1 Move pins, located in the center of the solenoid, inward until

they just contact the interlace gimbal plunger pads.

2 Ensure scanner is firmly mounted to reduce vibration effects to the greatest extent possible.

3 If necessary, remove the jumper between P1-5 and +5 Vdc to enable the scan and interlace drive amplifiers. Connect a jumper between +5 Vdc and J2-4 of the PCB to disable the interlace drive amplifier.

4 Once the scanner is mounted and connected as in Figure 3.4-25, turn power on. Cycling of power may be necessary to start the scanner. Ensure that the scanner is operating correctly at 60 Hz, which is accomplished as follows:

a Adjust R8 of the scan and interlace card for a scan frequency of 60 $\pm$ 0.5 Hz as measured at J2-7 of the PCB.

b Adjust R18 of the scan and interlace card for a spring limit pulsewidth of 2.45 $\pm$ 0.05 ms (widest of the two pulsewidths) as measured at J5 of the PCB.

c R8 and R18 interact with each other; therefore, it may be necessary to readjust R8 and R18 to achieve the pulsewidth and frequency as called out in steps a and b.

d Monitor the waveform at J4 of the scan and interlace card (Figure 3.4-26) with a scope. Adjust R32 so that the waveform during the active scan time is as nearly horizontal as possible.

e Remove PS-1 and connect PI-12 of the PCB to PI-12 of the scanner to enable the scan transducer bridge AGC voltage. Monitor the voltage at J7 of the PCB with a DVM. Adjust R122 on the scan and interlace card so that the voltage at J7 of the PCB is 1.9 $\pm$ 0.05 Vdc.

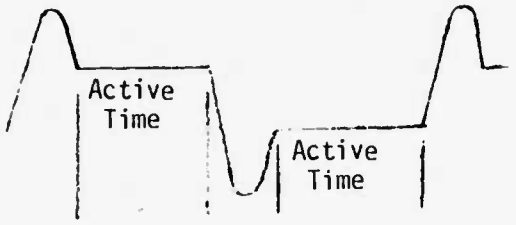


Figure 3.4-25. Scan Position Error Waveform

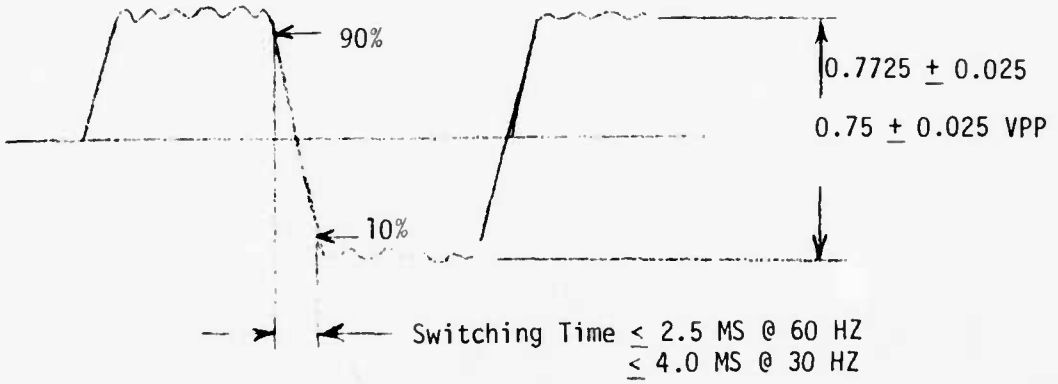


Figure 3.4-26. Interlace Signal

5 Remove the jumper between PI-5 and J2-4 of the PCB to enable interlaces. R111 (gain), R93 (drive), and R124 (balance) pots on the scan and interlace card must be adjusted to obtain the optimum interlace waveform (Figure 3.2-24) with total current drain from ±15 Vdc supplies of less than 450 MA.

6 Monitor the interlace waveform at J6 of the scan and interlace card with an oscilloscope. Adjust the interlace potentiometers R111, R93, and R124 of the PCB along with the solenoid stop pins to achieve the optimum interlace signal.

7 If at this time the scan angle of the mechanical scanner needs F-4 readjustments, perform the scan angle adjustment and steps 4 and 5 above.

3.4.4.1.6 Interlace Mode Adjustment

The two modes of interlace operation are a 2:1 mode (side or rear-mounted scanner) and a 1:1 mode. By shorting together the appropriate connector pins of the scan and interlace module, the interlace gimbal will be driven in either of the above modes. Table 3.4-VII indicates which pins (Figure 3.4-11) must be shorted together to achieve the above modes.

TABLE 3.4-VII

Interlace Mode Selection

2:1 Side	2:1 Rear	1:1
Short pin 31 to pin 33	Short pin 34 to pin 33	Short pin 33 to pin 32
Short pin 4 to pin 17	Short pin 4 to pin 17	Short pin 4 to pin 18
Pin 18 - no external connection	Pin 18 - no external connection	Pin 31 - no external connection
Pin 32 - no external connection	Pin 32 - no external connection	Pin 34 - no external connection
Pin 34 - no external connection	Pin 31 - no external connection	Pin 17 - no external connection

3.4.4.2 Video Electronics Adjustment

Due to the variations in gain for each module, a potentiometer adjustment has been provided to allow for adjustment of each channel to provide uniformity on the display. This adjustment is located on the postamplifier/control driver module and is set full maximum during the initial module test procedure.

When the video electronics is fully connected, then it should be balanced electronically by monitoring the output of the postamplifier/control driver module. After the electronic adjustment is performed, a finer alignment may be necessary when the display is viewed because the power output variations of the LED array were not included.

APPENDIX A

FLIR COMMON MODULE CHARACTERISTICS

This appendix provides additional descriptive material not already covered in the preceding system design sections.

A.1 Detector/Dewar

The sensor and dewar assembly common module (Figure A-1) performs the optical-to-electrical signal conversion function. A HgCdTe intrinsic photoconductive detector array of 180 elements sensitive in the 7.5 to 12 μm spectral region is used. Intrinsic photoconductive detectors operate by producing a change in conductivity when incident photons of sufficient energy excite a valence band electron in a semiconductor to the conduction band and produce an electron hole pair. The excited electrons and holes move within the semiconductor under the influence of an external electric field and produce an output current. The external electric field is created by a bias voltage supplied across the detector in series with a bias resistor. The signal is extracted by monitoring the voltage variation across the detector. The common module detectors, which exhibit a resistance of 50 ohms, are connected to 2000-ohm bias resistors contained in the detector/dewar modular assembly. These resistors are trimmed for signal channel balance. The detectors can be biased in groups of five when less than the full 180-element array is required by the system application.

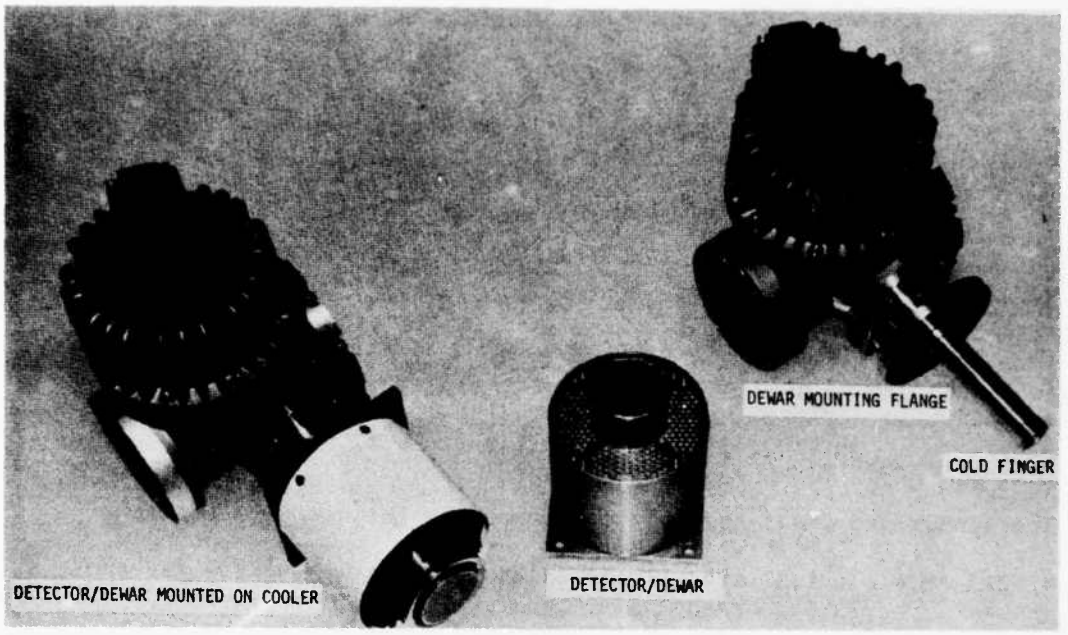


Figure A-1. Detector/Dewar

The dewar provides an insulated vacuum enclosure for maintaining low detector temperature and forms a cold shield which limits the detector FOV to an equivalent 75-degree cone. The cold shield limits the amount of background radiation seen by the detector from warm internal parts of the FLIR. The detector elements must be maintained at approximately 80°K during operation. At this temperature, thermal generation of conduction band electrons is minimal. The large number of thermally excited carriers at room temperature would normally dominate the signal created by incident photon-generated carriers. Similarly, incident photons from warm backgrounds both inside and outside the FLIR system create carriers. The noise associated with background photons may approach and exceed the signal. Thus, the dewar performs the dual function of insulating the detector to maintain low temperatures and

shielding it to minimize the detection of background radiation. Detector/dewar characteristics are shown in Table A-I.

TABLE A-I

Detector/Dewar Characteristics

Detector Material	HgCdTe
Number of Elements	180
Spectral Region	7.5 + 0.25 - 0.05 to 11.75 $\pm$ 0.25 μm
Time Constant	$\leq$2 μs maximum, 1 μs nominal
Detector Resistance	49 to 55 ohms (nominal at 80°K)
Detectivity (Detector temperature 80 +5, -20°K)	162 elements $\geq 3.4 \times 10^{10}$, 18 elements $\geq 2.0 \times 10^{0}$ cm $Hz^{\frac{1}{2}}$ W^{-1}
Responsivity	$\geq 2.0 \times 10^{4}$ V/W
Responsivity Variation	$\pm$40 percent
Bias Current*	I_{avg} = 4.5 mA I_{peak} = 8.0 mA
Bias Power	100 mW total
Detector FOV	75-degree cone
Heat Load (80 +5, -20°K)	0.4 watt (all elements operating)
Dewar Window Response at 50 percent transmission points	-7.5 +0.25, -0.05 μm -12.0 +0, -0.25 μm average transmission >85 percent
Size	See Figure 3.3-5
Detector/Dewar Assembly Weight	0.716 pound

*I_{AVG} = 2.5 mA from empirical data

A.2 Preamplifier

The preamplifier (Figure A-2) is extensively described in paragraph 3.4.1.1.2. Noise considerations are discussed in Appendix B.

A.3 Postamplifier/LED Driver

The basic functions of the postamplifier/LED driver (Figure A-3) are described in paragraph 3.4.1.1.3. Each channel contains two postamplifiers and one LED driver IC in series.

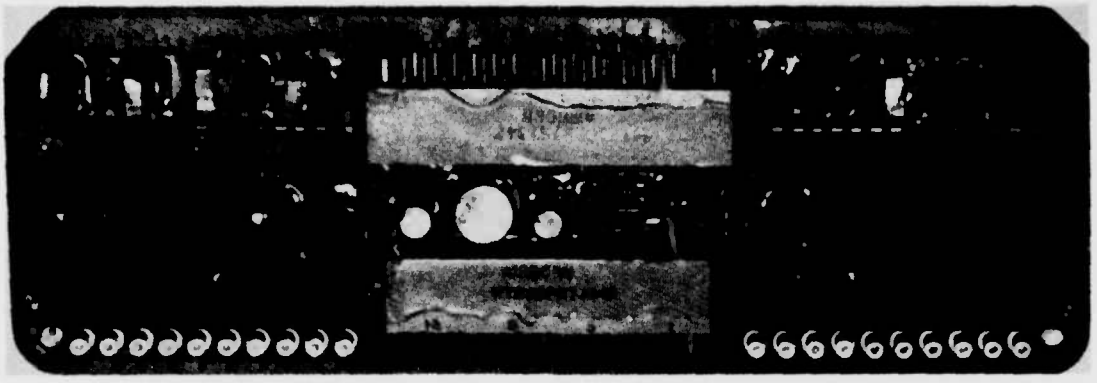
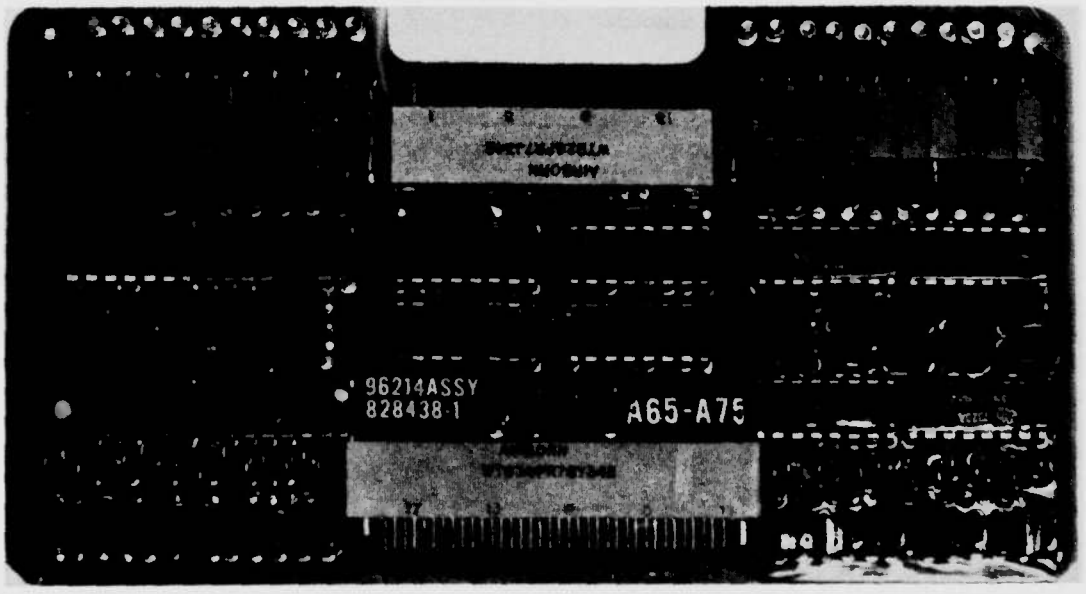


Figure A-2. Preamplitier



Fig[illegible] A-3. Postamplifier/Control Driver

A.3.1 Postamplifier IC Characteristics

Characteristics of the postamplifier IC are shown in Table A-II. The postamplifier IC contains five amplifiers as shown in Figure 3.4-18. All of the characteristics in Table A-II except the first four refer to each channel on a per-amplifier basis. The ambient temperature range of this IC is specified to be -54 to 95°C, and the maximum supply voltages are +15 Vdc and -15 Vdc for V_{CC} and V_{EE}, respectively.

TABLE A-11

Postamplifier IC Characteristics

V_{in}	Parameter	V_{gain} P7	V_{pol} P3	R_L (kΩ, each channel)	Mode*	V_{CC}	V_{EE}	Min	Max	Units
-	Positive Supply Current	Gnd	Gnd	∞	HP	+10.0	-10.0	7.0	11.0	mA
-	Negative Supply Current	Gnd	Gnd	∞	HP	+10.0	-10.0	-6.0	-13.0	mA
-	Positive Supply Current	Gnd	Gnd	∞	LP	+6.0	-6.0	4.0	6.5	mA
-	Negative Supply Current	Gnd	Gnd	∞	LP	+6.0	-6.0	-4.0	-7.0	mA
-	dc Output Voltage	Gnd	-0.2V	5	I	+10.0	-10.0	2.5	7.5	Vdc
-	dc Output Voltage	Gnd	-4.7	5	N	+10.0	-10.0	2.5	7.5	Vdc
-	dc Output Voltage	Gnd	-0.2	5	I	+6.0	-6.0	1.25	3.25	Vdc
-	dc Output Voltage	Gnd	-2.8	5	N	+6.0	-6.0	1.25	3.25	Vdc
+50 mV	Output Voltage Swing	Gnd	Gnd	5	I	+6.0	-6.0	-750	-	ΔmV
-50 mV	Output Voltage Swing	Gnd	Gnd	5	I	+6.0	-6.0	+750	-	ΔmV
+50 mV	Output Voltage Swing	Gnd	-2.8	5	N	+6.0	-6.0	+750	-	ΔmV
-30 mV	Output Voltage Swing	Gnd	-2.8	5	N	+6.0	-6.0	-750	-	ΔmV
10 mV p-p	Voltage Gain (1 kHz)	Gnd	Gnd	5	I	+6.0	-6.0	70	90	V/V
-	Input Resistance (1 kHz)	Gnd	Gnd	5	I	+6.0	-6.0	7500	12500	Ohms
-	Output Resistance	Gnd	Gnd	5	I	+6.0	-6.0	100	400	Ohms
-	High Frequency Response	Gnd	Gnd	5k/200 pf	I	+6.0	-6.0	1.0	-	MHz
10 mV p-p	Channel Crosstalk (1 kHz)	Gnd	Gnd	5	I	+6.0	-6.0	-	-40	dB
-	White Noise (Resistance = 1 kΩ; bandwidth = 5 Hz to 35 kHz)	Gnd	Gnd	5	I	+6.0	-6.0	-	50	$nV/\sqrt{Hz}$
-	Slew Rate (no distortion)	Gnd	Gnd	5	I	+6.0	-6.0	500	-	1 kHz
-	Rise Time	Gnd	Gnd	5	I	+6.0	-6.0	-	260	ns
-	Fall Time	Gnd	Gnd	5	I	+6.0	-6.0	-	300	ns
-	Overshoot	Gnd	Gnd	5	I	+6.0	-6.0	-	10	Percent
-	Overload Recovery	Gnd	Gnd	5	I	+6.0	-6.0	-	50	μs

*I = inverting, N = noninverting

A.3.2 LED Driver IC Characteristics

The LED driver IC contains five LED drivers per 16-pin, dual in-line package and is a closed-loop amplifier with a gain of 6. The characteristics are shown in Table A-III.

TABLE A-III

LED Driver IC Characteristics

Parameter	V_{gate} (Vdc)	R_L (ohm)	ein (V p-p)	Limits Min	Limits max	Units
Positive Supply Current	-0.4	-	-		12.0	mA
Negative	-0.4	-	-		10.0	mA
dc Output Voltage	-0.4	150	-	2.300	2.450	Vdc
dc Output Voltage	-1.0	150	-	5.825	5.975	Vdc
Input Resistance @ 1 kHz	-0.8	-	0.1	6500	10000	Ohms
Voltage Gain @ 1 kHz	-0.7	150	0.5	5.75	6.05	V/V
High-Frequency Response	-0.7	150	-	350	-	kHz
Low-Frequency Response	-0.7	150	-	0.48	-	Hz
Channel Crosstalk @ 1 kHz	-0.7	150	-	0.5	-40	dB
Slew Rate (no distortion)	-0.7	150	1.0	200	-	kHz
Rise Time	-0.7	150	1.0	1.0	1.0	µs
Fall Time	-0.7	150	1.0	1.0	1.0	µs
Overshoot	-0.7	150	1.0	-	5	Percent
Overload Recovery	-0.7	150	0.4	-	50	µs
Voltage Gain versus Temperature @ 1 kHz	-0.7	150	0.87	-	± 5	Percent

Conditions: V_{CC} = +10 Vdc
V_{EE} = -10 Vdc
V_d = +10 Vdc

The LED driver has an input called dc restore which is available at the IC level to be used to clamp the video input to ground by inserting a positive level (+5 Vdc) for the clamp condition and a negative level for the normal mode condition. This function is not presently brought out to the postamplifier/control driver module connector.

Operating temperature for the IC is specified over the range from -54°C to 95°C. The maximum values for V_{CC} and V_{EE} are +18 and -18 Vdc, respectively. The maximum peak and average output currents are specified to be 50 and 25 mA, while the input voltage range is specified to be 0 to -2.5 Vdc.

The postamplifier/LED driver provides an externally controlled gain for the video signal, which can be adjusted by a system operator to optimize image quality. The gain control function is achieved in the postamplifier IC by controlling the emitter resistances of a differential amplifier. The controlling function is an externally controlled voltage produced by the auxiliary control PCB, which is translated into a controlled current source in the postamplifier IC. Since the postamplifier gain is temperature sensitive, a temperature compensation network has been provided in the auxiliary control to limit the drift in gain due to temperature change.

Postamplifier/auxiliary control PCB tests at overtemperature have demonstrated that the temperature compensation network provides adequate compensation over only a small range of gain control voltages. An analysis of the postamplifier/LED driver gain characteristics using the simplified schematic of Figure 3.4-6 demonstrates that the gain is a complex function of gain and voltage as follows:

$$\text{Gain} = \frac{11{,}358.7(V_{G1}(T)+/V_{EE}/-V_{EE}/-V_{BE}(T))(V_{G2}(T)+/V_{EE}/-V_{BE}(T))(/V_{EE}/-V_{BE(T)})^2}{(0.005415\ T\ [/V_{EE}/-V_{BE}(T)] + \frac{k}{q}\ T^2)^2}$$

where:

$V_{G1}(T)$ = auxiliary control gain 1 voltage as a function of temperature

$V_{G1}(T) = V_{G1} + 0.011\ V/°C \times (T-298)$

V_{G1} = ambient temperature (298°K) gain voltage

T = temperature in °K

$V_{G2}(T)$ = auxiliary control gain 2 voltage as a function of temperature

$V_{G2}(T) = V_{G2}$

$V_{BE}(T) = V_{BE} + TC \times (T-298)$

V_{BE} = V_{BE} at 298°K and was found to be 0.54 empirically

TC = temperature coefficient and was found to be -0.0075 V/°C empirically

$/V_{EE}/$ = absolute value of negative supply voltage

k = Stefan-Boltzman constant

q = electron charge.

Figure A-4 is a computer printout of absolute postamplifier gain as a function of gain control voltages and as a function of temperature. Gains 1 and 2 are the room temperature gain control voltages, gain HT is the gain at 71°C, gain RT is the gain at room ambient (25°C), and gain LT is the gain at -54°C. Change H and change L are the high- and low-temperature gains normalized to room ambient gain for the given gain control settings. The temperature compensation circuit of the auxiliary control has a positive TC of 11 mV/°C. The columns Change TC H and Change TC L indicate the change in volts/°C required in the auxiliary control TC to exactly compensate high-temperature gain and low-temperature gain. Note that the data closely follow the results obtained from the 15 postamplifier PCBs run at over-temperature.

Vee= 4.25

GAIN 1	GAIN 2	GAIN H T	GAIN R T	GAIN L T	CHANGE H	CHANGE L	CHANGE TC H	CHANGE TC L
-3.0	-3.0	812	471	-33	1.722	-.041	-.0083	.0015
-3.0	-2.0	1555	1100	-248	1.412	-.159	-.0057	.0017
-3.0	-1.0	2297	1730	-462	1.327	-.201	-.0043	.0018
-3.0	.0	3039	2359	-676	1.288	-.222	-.0044	.0018
-3.0	1.0	3781	2988	-891	1.265	-.235	-.0041	.0019
-3.0	2.0	4524	3617	-1105	1.250	-.244	-.0039	.0019
-3.0	3.0	5266	4246	-1319	1.240	-.250	-.0039	.0019
-2.0	-3.0	1459	1100	249	1.326	.171	-.0102	-.0092
-2.0	-2.0	2793	2568	1036	1.087	.657	-.0033	-.0038
-2.0	-1.0	4126	4036	3423	1.022	.829	-.0009	-.0018
-2.0	.0	5459	5504	5010	.991	.917	.0003	-.0009
-2.0	1.0	6792	6972	6597	.974	.971	.0010	-.0003
-2.0	2.0	8126	8440	8184	.962	1.003	.0016	.0000
-2.0	3.0	9459	9908	9771	.954	1.032	.0019	.0003
-1.0	-3.0	2107	1730	533	1.217	.253	-.0113	-.0177
-1.0	-2.0	4031	4036	3921	.998	.972	.0000	-.0006
-1.0	-1.0	5955	6343	7309	.938	1.227	.0041	.0054
-1.0	.0	7879	8650	10698	.910	1.357	.0061	.0095
-1.0	1.0	9803	10957	14086	.894	1.436	.0074	.0104
-1.0	2.0	11728	13263	17474	.884	1.480	.0082	.0116
-1.0	3.0	13652	15570	20862	.876	1.508	.0089	.0105
.0	-3.0	2754	2359	817	1.167	.296	-.0121	-.0256
.0	-2.0	5269	5504	6006	.957	1.139	.0037	.0051
.0	-1.0	7784	8650	11196	.899	1.438	.0094	.0159
.0	.0	10299	11795	16385	.873	1.590	.0123	.0215
.0	1.0	12814	14941	21575	.857	1.683	.0141	.0249
.0	2.0	15330	18087	26764	.847	1.745	.0152	.0272
.0	3.0	17845	21232	31953	.840	1.790	.0161	.0288
1.0	-3.0	3401	2988	1101	1.138	.323	-.0129	-.0333
1.0	-2.0	6507	6972	8091	.933	1.243	.0076	.0119
1.0	-1.0	9613	10957	15082	.877	1.568	.0140	.0279
1.0	.0	12719	14941	22073	.851	1.735	.0186	.0361
1.0	1.0	15825	18925	29063	.836	1.836	.0209	.0410
1.0	2.0	18932	22910	36054	.826	1.904	.0224	.0444
1.0	3.0	22038	26894	43045	.819	1.953	.0235	.0469
2.0	-3.0	4048	3617	1394	1.119	.342	-.0136	-.0406
2.0	-2.0	7745	8440	10176	.917	1.313	.0115	.0193
2.0	-1.0	11442	13263	18068	.862	1.657	.0204	.0406
2.0	.0	15139	18087	25960	.837	1.833	.0250	.0515
2.0	1.0	18837	22910	33852	.822	1.940	.0277	.0583
2.0	2.0	22534	27733	41744	.812	2.013	.0296	.0635
2.0	3.0	26231	32556	49636	.805	2.064	.0309	.0667
3.0	-3.0	4695	4246	1679	1.105	.355	-.0143	-.0429
3.0	-2.0	8993	9908	12261	.908	1.364	.0134	.0231
3.0	-1.0	13291	15570	22854	.853	1.722	.0260	.0537
3.0	.0	17589	21232	33447	.828	1.909	.0314	.0673
3.0	1.0	21888	26894	44041	.813	2.015	.0347	.0756
3.0	2.0	26186	32556	54634	.805	2.088	.0369	.0811
3.0	3.0	30424	38219	65227	.796	2.143	.0384	.0851

Figure A-4. Absolute Postamplifier Gain As Function of Gain Control Voltage and Temperature

The computer analysis indicates the following points of interest:

1 The auxiliary control compensates the postamplifier over a small range of control voltages as indicated by the brackets.

2 The auxiliary control can be made to compensate the postamplifier only at gain control settings in which change TC H = change TC L ± 2 mV/PC. This can be accomplished by changing R31 on the auxiliary control.

3 The analysis shows that, at low temperature, the gain becomes negative at minimum gain on gain 1. This indicates the amplifier has been driven to cutoff, which has been experimentally verified.

4 Required temperature compensation is not a function of absolute gain but is related to the interaction between first and second stage gain.

5 There is no linear temperature compensation circuit that will compensate the postamplifier over a wide range of gain control settings.

6 The temperature compensation points using the auxiliary control are also a function of the negative IC supply voltage.

A.3.3 Technical Characteristics

Table A-IV lists the module characteristics required by the development specification at room temperature unless otherwise specified.

Empirical data were measured on the postamplifier/control driver to identify characteristics that might be important for the broad range of applications for the FLIR system. These data are:

1 The polarity input current was measured and the equivalent resistance to the negative supply was found to be approximately 3.27 kΩ (pin 28 to pin 27) for the complete module.

2 Both of the currents for gain command 1 and gain command 2 were measured. The equivalent resistance to the negative supply for the complete module was between 4.5 and 5.0 kΩ (pin 12 to pin 27, pin 29 to pin 27).

3 Measurements were made to determine the change in output voltage for a change in gain command. These averaged test results of all 20 channels of one complete module are reflected in Table A-V. The gain control range for all the channels combined was greater than 15 dB worst case. Because each module has two postamplifier ICs, the total range of 30 dB gain control can be accepted as a realistic requirement.

4 A cursory check was made to determine the effect on gain versus gain command voltage variation of V_{EE}. As might be expected, the gain control decreases as the negative supply increases. The amount of decrease in gain control is approximately equal to the ratio of the new V_{EE} to that used in Table A-V (i.e., if V_{EE} were chosen to be -6V, and the change in E_o for -2V were $\Delta E_o = 0.336$, the new change would be $\Delta E_o' = 0.336 \times \frac{-3.47}{-6} = 0.194$ volts). Actual measurements demonstrated this approximation to be accurate within ±15 percent and in most cases less than ±10 percent.

A.4 Auxiliary Control

The auxiliary control module (Figure A-4) is described in paragraph 3.4.1.1.4. The technical characteristics shown in Table A-VI correspond with the development specification at 25°C, unless otherwise specified.

TABLE A-IV

Postamplifier/Control Driver Characteristics

Parameter	Characteristics	Comments
Supply voltage, current, and ripple (LP)	+4.8 @ 60 mA; 100 mV ripple -4.8 @ 30 mA; 100 mV ripple +7.0 @ 30 mA; 100 mV ripple -3.5 @ 35 mA; 0.2 mV ripple +3.5 @ 35 mA; 0.2 mV ripple	LP mode, average voltage and current, rms ripple
Supply voltage, current, and ripple (HP)	10.0 @ 140 mA; 100 mV ripple -6.75 @ 35 mA; 50 mV ripple -4.25 @ 45 mA; 0.2 mV ripple +4.25 @ 45 mA; 0.2 mV ripple	HP mode, average voltage and current, rms ripple Pin 30 open
Polarity	+0.6 ± 0.25 Vdc, -3.5 ± 1.25 Vdc	+0.6V is minimum
Gain Control	30 dB	Gain command 1 and gain command 2
Low-Frequency Cutoff*	6 ± 2 Hz	
High-Frequency Cutoff*	110 ± 40 kHz	
Voltage Gain*	10,000 V/V to 18,000 V/V	Programmable
Input Impedance*	10 ± 2.5 kΩ	
Output Current*	10 ± 3 mA	Load is a resistor in series with a LED
Output Impedance*	205 ± 10 ohms	
Recovery Time*	0.2 seconds	Paragraph 3.4.1.1.2.4
ac Gain Balance*	15 dB	Provided for by potentiometer in each channel
Channel-to-Channel Tracking	± 5 percent ± 10 percent ± 15 percent	0°C to 55°C 55°C to 71°C -54°C to 0°C
Voltage Gain Drift	± 10 percent ± 15 percent	0°C to 71°C -54°C to 0°C
Gain Tracking Error	± 5 percent ± 5 percent ± 10 percent	Over 30 dB gain control range at room temperature 0°C to 55°C -54°C to 0°C, 55°C to 71°C

*Refers to each channel of the module.

TABLE A-V

Gain Command Measurements

Gain Command 1 Voltage (Vdc)	ΔE_o (Vrms) Max	Nom	Min	ΔE_o (dB) Max	Nom	Min
-2.0	0.336	0.297	0.283	-9.47	-10.54	-10.96
-1.0	0.715	0.645	0.622	-2.91	- 3.81	- 4.12
0.0	1.0	1.0	1.0	0.0	0.0	0.0
+1.0	1.36	1.34	1.30	2.67	2.54	2.28
+2.0	1.69	1.67	1.65	4.56	4.35	4.35
+3.0	2.04	2.00	1.96	6.19	6.00	5.84

E_o = 1 Vrms V_{CC} = 3.41 Vdc V_{EE} = 3.47 Vdc V_{IR} = -0.116 Vdc

TABLE A-VI

Auxiliary Control Characteristics

Parameter	Characteristic		Comments
Supply Voltage		+10 ± 0.2 Vdc	HP mode
		-7.5 ± 0.2 Vdc	HP mode
		+4.8 ± 0.1 Vdc	LP mode
		-4.8 ± 0.1 Vdc	LP mode
		+7.0 ± 0.1 Vdc	LP mode
		-7.0 ± 0.1 Vdc	LP mode
Current Requirements (HP mode)	Unloaded	33 mA max	+10 Vdc, regulator current
	Loaded	660 mA max	
	Unloaded	24 mA max	-7.5 Vdc, regulator current
	Loaded	660 mA max	
Current Requirements (LP mode)	Loaded	540 mA max	+4.8, postamplifier current
	Unloaded	540 mA max	-4.8, postamplifier current
	Loaded	15 mA max	+7.0, regulator current only
	Unloaded	15 mA max	-7.0, regulator current only
IR Level		+1.0V	Nominal positive level
		0 to -1.5V	Nominal negative level; this is variable as brightness is controlled.
IR Gain Command Voltage		-3.0 to +3.0 Vdc	Gain command 1, range nominal
(HP mode)		-3.0 to +3.0 Vdc	Gain command 2, range nominal
(LP mode)		-2.0 to +2.0 Vdc	Gain command 1, range nominal
		-2.0 to +2.0 Vdc	Gain command 2, range nominal
Positive Regulator Output Range (HP mode)		3.0 to 4.5 Vdc	Supplies post-amplifiers of postamplifier/ control driver
(LP mode)		+2.5 to +3.5 Vdc	
Negative Regulator Output Range (HP mode)		-3.0 to -4.5 Vdc	Supplies post amplifiers of postamplifier/ control driver
(LP mode)		-2.5 to -3.5 Vdc	
IR Polarity Control		+0.6 ± 0.25 Vdc -3.5 ± 1.5 Vdc	Positive level Negative level
Polarity Transient Suppression		140 ± 40 ms	Provides a +1.0 Vdc level at pin 10 of auxiliary control module
Scan Failure Protect		1.0 Vdc	Nominal voltage without rectangular waveform at pin 12 of the module

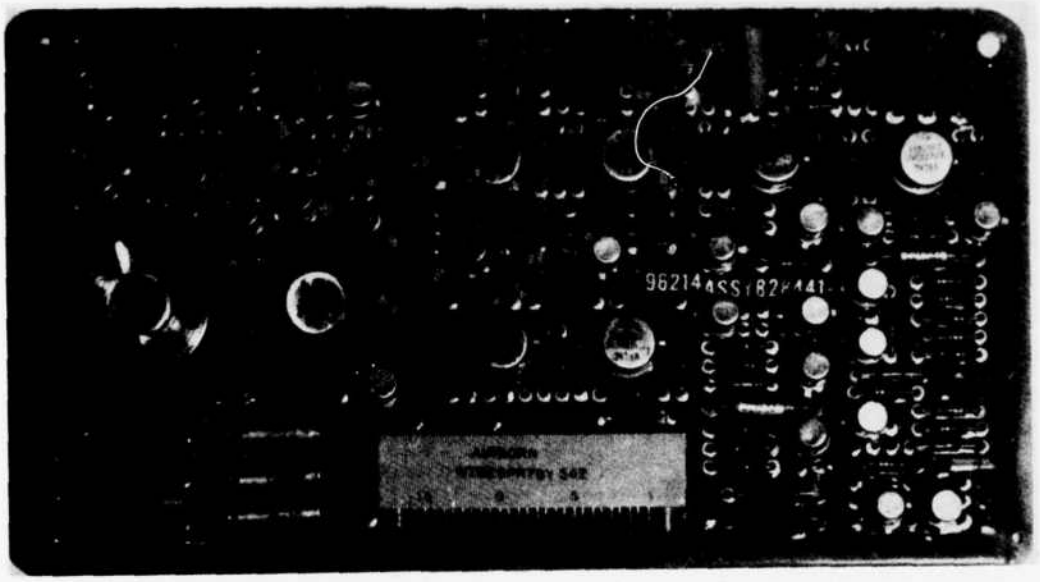


Figure A-4. Auxiliary Control

A.5 Bias Regulator

The bias regulator module (Figure A-5) is described in paragraph 3.4.1.1.5. Characteristics are provided in Table A-VII. Unless otherwise specified these characteristics are for an ambient temperature of +23 $\pm$2°C.

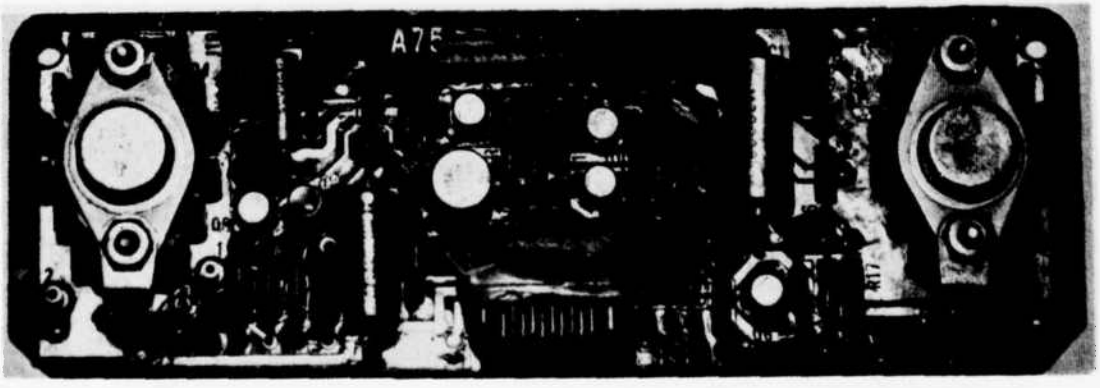


Figure A-5. Bias Regulator

TABLE A-VII

Bias Regulator Characteristics

Parameter	Characteristic
*Input voltage	+9.5 to +10.0 Vdc
Output current	1.08 amperes, maximum
Output voltage	
+23 ±2°C	+5 ±0.2 Vdc
-54 to +71°C	+5 ±0.5 Vdc
Current limit	1.5 ±0.25 amperes
Line rejection	>50 dB to 50 kHz
Output impedance	<0.3 ohm to 50 kHz

*Analysis has indicated that from 10 to 11 Vdc is a preferred value to prevent the bias regulator from saturating and consequently coupling any ripple of the bias regulator directly to the bias input of the detector/dewar module.

A.6 Scan and Interlace

The scan and interlace module (Figure A-6) provides the following functions:

1. Control of the frequency and position of the mechanical scan mirror
2. Solenoid drive information for the interlace gimbal of the mechanical scanner
3. Control of interlace phasing and scan direction
4. Detection of mechanical scan failure which disables the scan power amplifier

5 External synchronization capability

6 A video gate signal which may be used to blank video information during scan mirror turnaround.

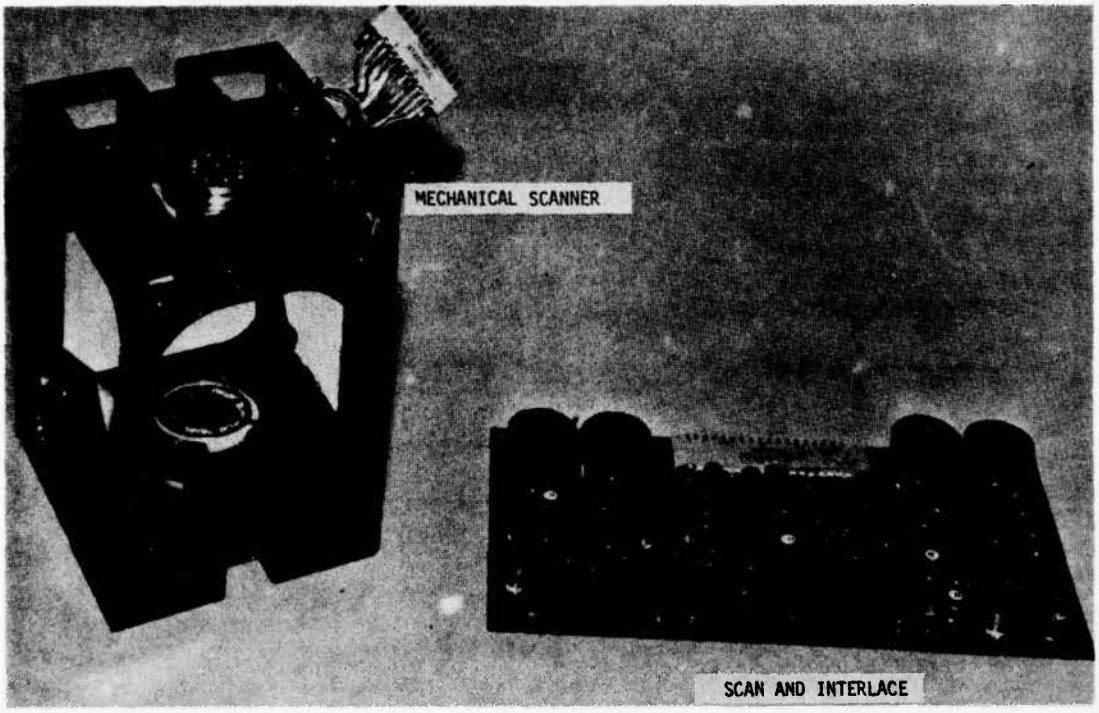


Figure A-6. Scan and Interlace and Mechanical Driver

A.6.1 Scan Position Control Loop

The scan mirror is directly coupled to the two torque motors, one each on the lower and upper ends of the gimbal. An extension of the bottom scan mirror trunnion contacts the return springs at each end of the active scan. The return springs act as energy-absorbing elements for the scan axis, storing energy from the motion in one direction and restoring that energy to the scan mirror in the opposite direction.

The azimuth position of the scan mirror is controlled by the scan position control loop on the 60 Hz scan and interlace card (Figure A-7).

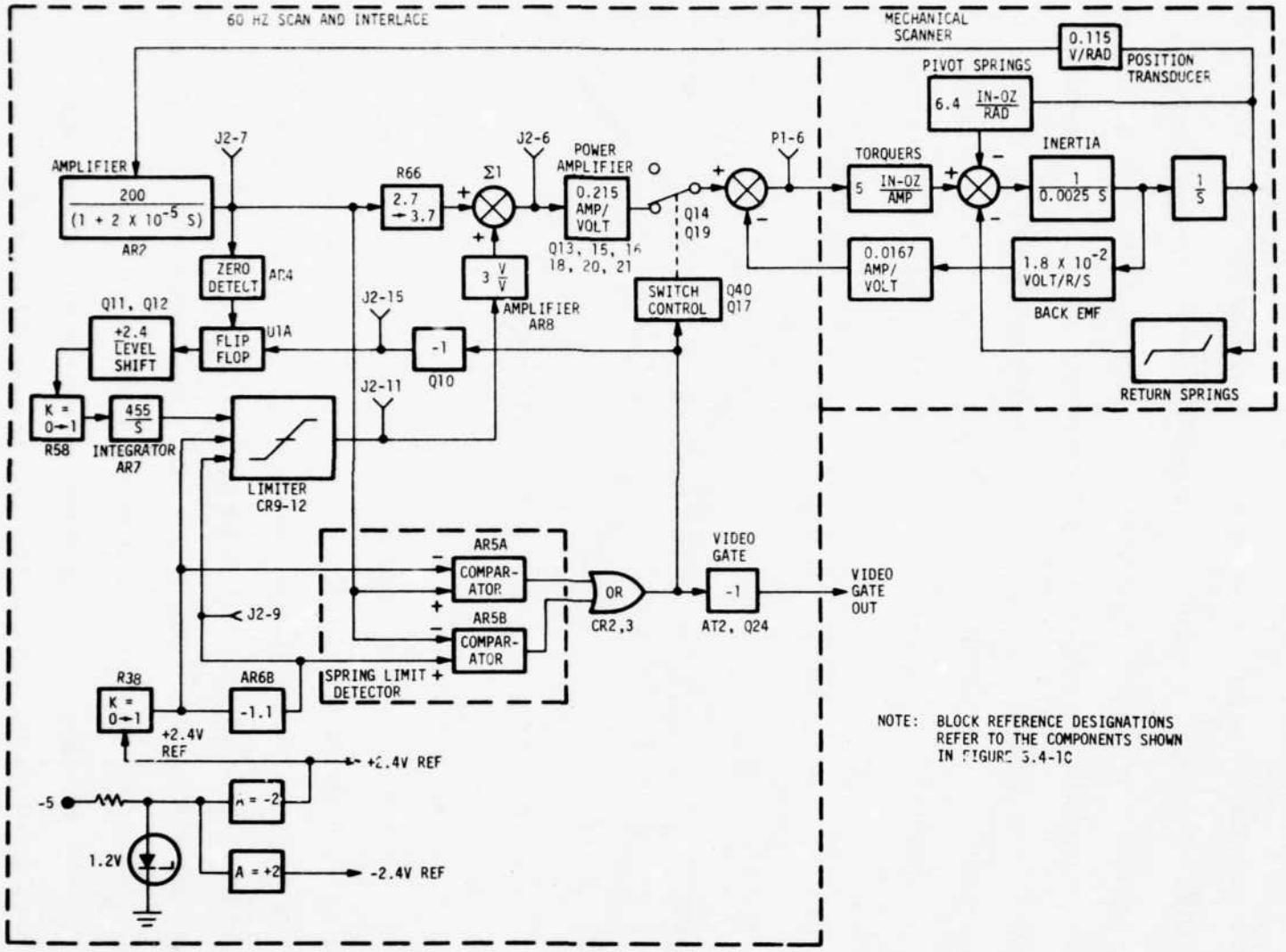


Figure A-7. Scan Position Control Loop

A modified triangular waveform shown in Figure A-8 is used as a reference signal (J2-11) and is generated by the integrator AR1 and limiter CR9-CR12. This signal is amplified and compared at the summing junction (Σ1) with the amplified scan position transducer output at J2-7. For the proper operation of the loop, these two signals must be equal and out of phase. R66 is an adjustment that allows for compensation of the initial tolerance of various error contributors. If an imbalance occurs at the junction, then the remainder of the loop will respond to correct for the imbalance.

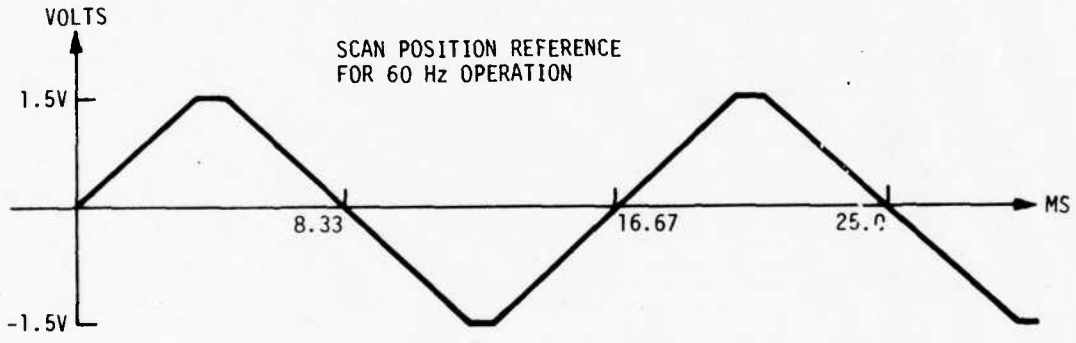


Figure A-8. Scan Position Reference Waveform

Both the positive and negative limits of the reference integrator are set by R38 which also sets the limits over which the power amplifier will operate. When the amplified position signal from the transducer exceeds the limits set by the spring limit detector AR5A and AR5B, the power amplifier is disabled. The output of an OR gate (CR2, CR3) will go high when either spring limit is exceeded by the amplified position signal. With the power amplifier disabled, the mirror will continue to move and depress one set of return springs. The energy stored within the springs will cause the mirror to return in the opposite direction causing the OR gate output to go low when the position level is within the range set by the spring limit

detector. When this happens, the level on the input of the integrator (AR7) changes from positive to negative, causing the integrator to begin integrating in the opposite direction. This keeps the scan mirror moving in a linear fashion. The frequency at which the scan mirror operates is determined by the setting of R58 which controls the input level to the integrator. This determines the rate of integration and, thus, the rate of scan mirror movement. The +2.4 and -2.4 Vdc regulators are required to maintain voltage and timing levels within acceptable operating range limits.

Another function derived from the scan position loop is the signal required to cause blanking of the video during interlace time. This function is performed by the output of pin 20 of Figure 3.4-10 and is optically isolated so that ground isolation of the video electronics may be maintained.

A.6.2 Transducer Gain Regulator Loop

The transducer gain regulator loop shown in Figure A-9 provides the basic function of maintaining the output of the transducer amplifier AR2 at a constant fixed voltage of 3.8 volts peak to peak (1.9 volts peak). This compensates primarily for the variations in transducer gain with time and temperature.

The signal out of the scan position transducer located within the mechanical scanner varies directly with the voltage applied to the transducer bridge circuit. The output of the error amplifier (AR1, Q1) is the voltage applied to both the scan position and interlace position transducer bridge circuits. The signal generated at the scan transducer by movement of the scan mirror is amplified by the inverting amplifier AR2, the output of which is rectified and peak detected by Q4 and C4 to generate a dc level. The

difference between this dc level and the voltage set by the wiper of R16 is amplified by the error amplifier (AR1, Q1) and adjusts the loop to maintain the voltage output from the scan position transducer amplifier constant. Initially the voltage across the scan transducer is set tc approximately 1.9 volts by R16 of the 60 Hz scan and interlace module.

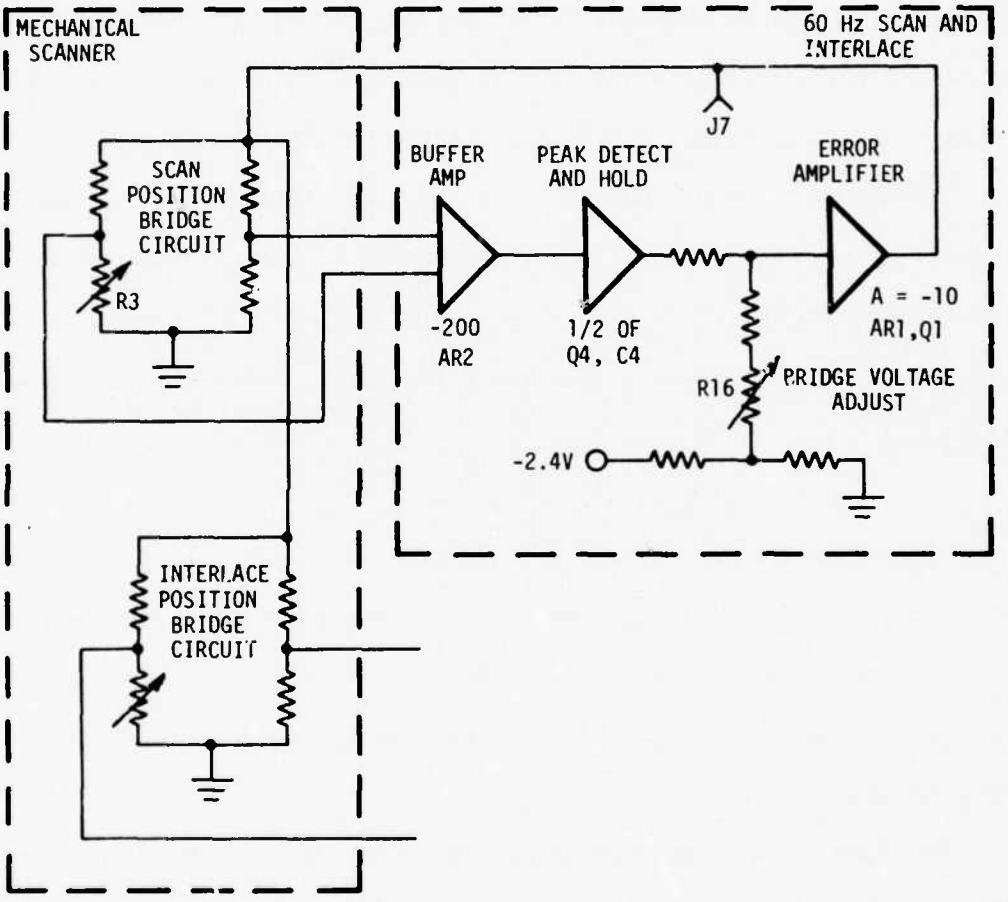


Figure A-9. Transducer Gain Regulator

A.6.3 Interlace Position Control Loop

The circuitry of Figure A-10 is available on the 60 Hz scan and interlace card and controls the interlace function, which occurs at the end of each azimuth scan or at the end of every other azimuth scan for 2:1 or 1:1

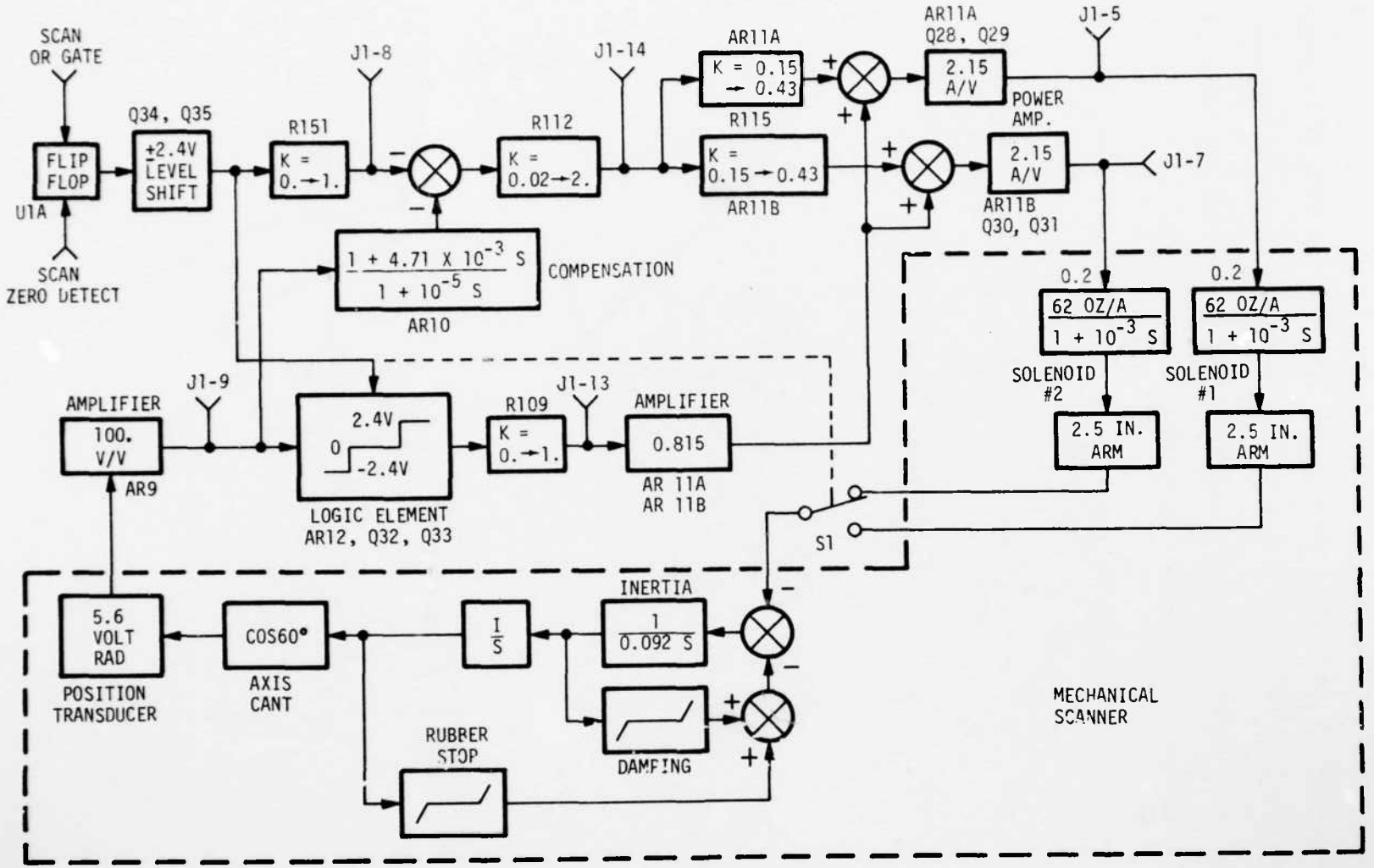


Figure A-10. Interlace Position Control

interlace, respectively. While in the 2:1 interlace mode, it is possible to operate in either side or rear scan phasing. Figure A-11 represents the phase relationships between the scan and interlace transducer outputs for various modes of interlace operation.

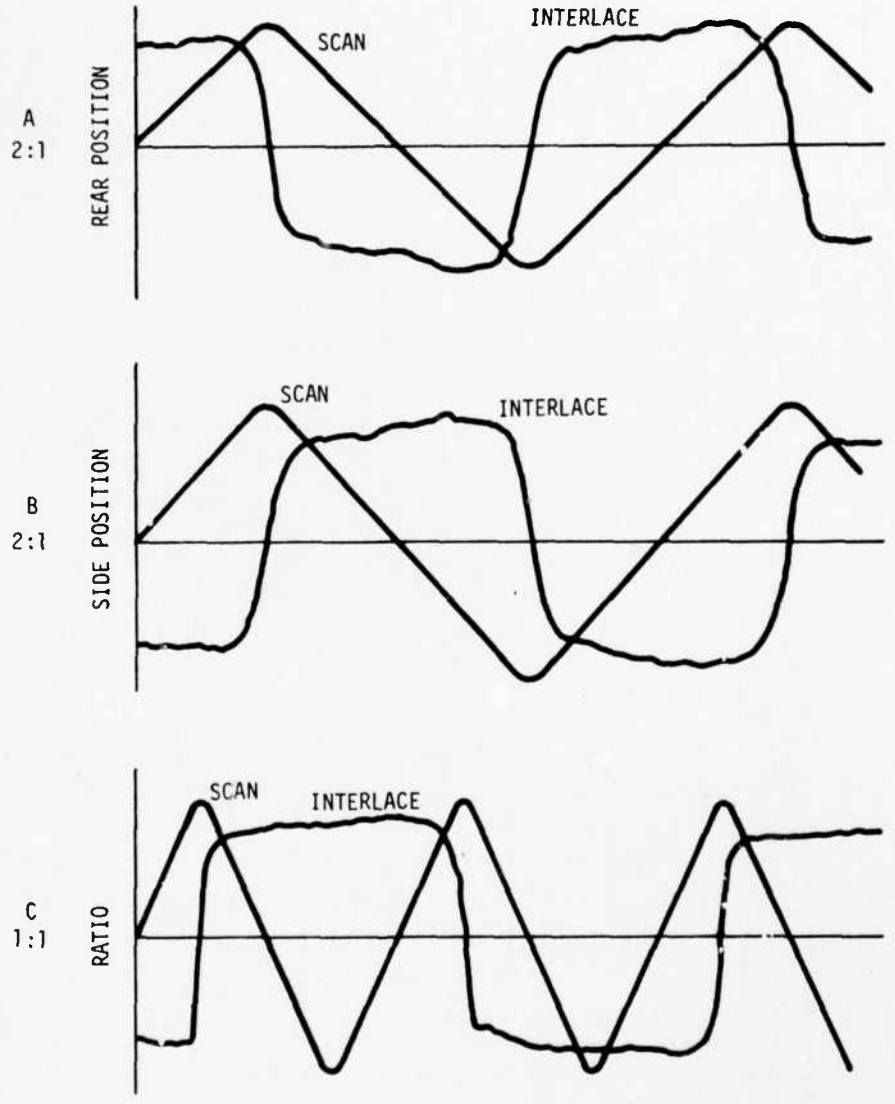


Figure A-11. Interlace Transducer Output Phase Relationships

In the 2:1 rear interlace mode of operation, the interlace gimbal is held in position by solenoid 1 which is driven by the current amplifier 1 (AR11A, Q28, and Q29). At the end of the azimuth scan, interlace action occurs and the output of the +2.4-volt level shifter (Q34, Q35) changes state, causing the interlace circuitry to turn solenoid 1 off and solenoid 2 on. Simultaneously, the output of the logic element (AR12, Q32, Q33) will change from zero volts to 2.4 volts. This signal produces an initial starting current for solenoid 2 which previously had been deenergized. The interlace gimbal will now start to move as directed by the plunger of solenoid 2. The interlace transducer then detects this motion and couples electrical signals to amplifier AR9. When the output of the interlace position transducer amplifier (AR9) indicates that the interlace gimbal has gone halfway through its interlace motion, the high current producing signal from the logic element will go to zero volts. The output signal from the level shifter will continue to maintain current through solenoid 2 and sustain the interlace motion.

As the interlace gimbal rate increases, the compensating network associated with AR10 will cause the current driver (AR11A, Q28, Q29) and solenoid 1 to become energized. This has the effect of slowing down the interlace gimbal motion, before the solenoid stops are reached. As the interlace gimbal slows down, the effects of the compensating network decrease until finally the interlace gimbal has reached the solenoid stops. At this point solenoid 2 is the only solenoid energized and will be held in this position by the signals from the 2.4-volt level shifter (Q34, Q35) and the output of AR9 by the current amplifier AR11B, Q30, Q31.

A.6.4 External Synchronization Loop

The 60 Hz scan and interlace card has the ability to accept an external synchronization input signal (such as a 60 Hz TV vertical synchronization pulse) as shown in Figure A-12. An optical isolator AT1 is used for the external synchronization input which provides ground isolation, the output of which is used to drive the one-shot device (U2A). R145 of U2A is adjusted to cause the output of U2B to become phase-locked with the output of the zero crossing detector AR4 of the scan position control loop. The output of U2B is adjusted for a 50 percent duty cycle using R146. These two outputs (AR4, U2B) are forced to be equal in duty cycle. When this occurs, the input from the level shifter (Q9, Q39) has no effect on the integrator AR7. If the two signals from the level shifter are not equal, the rate of the integrator would then increase or decrease as required to adjust the speed of the scan mirror so that the output signal from the zero crossing detector (AR4) would be of equal time duration to the signal at U2B. When this occurs the scan frequency is then synchronized to the external signal.

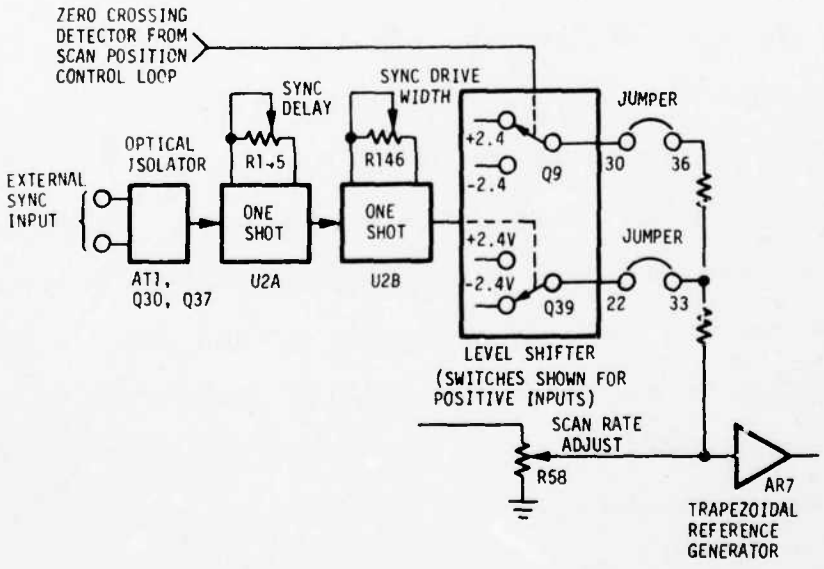


Figure A-12. External Synchronization Circuit

A.6.5 Characteristics

Unless otherwise specified, the characteristics given in Table A-VIII are for ambient temperature of 23 ±2°C.

TABLE A-VIII

Scan and Interlace Characteristics

Parameter	Characteristics
Scan Frequency Range	20 frames/40 fields per second to 62 frames/ 124 fields per second
Frequency Drift	≤+10, ≥-10 percent of ambient setting
Interlace Modes	2:1 side, 2:1 rear, 1:1
Power Supply Input*	+5.0 ±0.3V @ 1.0A peak (0.65W max) -5.0 ±0.3V @ 1.0A peak (0.25W max) +15.0 ±0.5V @ 1.5A peak -15.0 ±0.5V @ 1.5A peak } total 6.6W max
Ripple	±5.0 Vdc supplies; 0.1V p-p max ±15.0 Vdc supplies; 0.2V p-p max
Supply Rise Time	0.5s max
Supply Tracking	±15 Vdc turn on rise time ≤ +5, ≥ -5 Vdc turn on rise time ±5 Vdc will track within 20 percent
Supply Impedance	≤ 0.1 ohm to 10 kHz and ≤ 5 ohm to 100 kHz
Scan Efficiency	≥ 70 percent for scan angles up to 10 degrees and for scan frequencies between 20 and 62 Hz
Scan Jitter in Azimuth	≤ 0.75 mrad for scan angles up to 10 degrees and for scan frequencies between 20 to 62 Hz
Scan Jitter in Interlace	±10 percent over central 80 percent area of active scan ±15 percent of initial setup over temperature (soak @ -62°C, operate at -30°C)
Video Gate	Provide isolated current sink of 2.0 mA
Scan Failure	Disable power amplifier to both scan motors and disable both solenoids when scan mirror stops

*For 20 to 30 Hz operation, the ±15 Vdc supplies may be reduced to ±5 Vdc and the total power required will be ≤ 4.0 watts maximum.

A.7 Inverter

The dc/ac inverter (Figure A-13) converts 24 Vdc to 400 Hz, 115 Vac to drive the cooler motor. The module is housed in a metal enclosure containing two printed circuit cards and a heat sink assembly. The first card (A1, square wave generator) shown in Figure A-14 provides initial signal generation, pulse shaping, amplification, and current overload protection. The second card (A2, 24-volt power board) shown in Figure A-15 provides power driver transformer circuits, phase shifting control for the cooler module, and a current sensing circuit. The heat sink assembly provides power drivers for the output transformer and phase shifting capacitors.

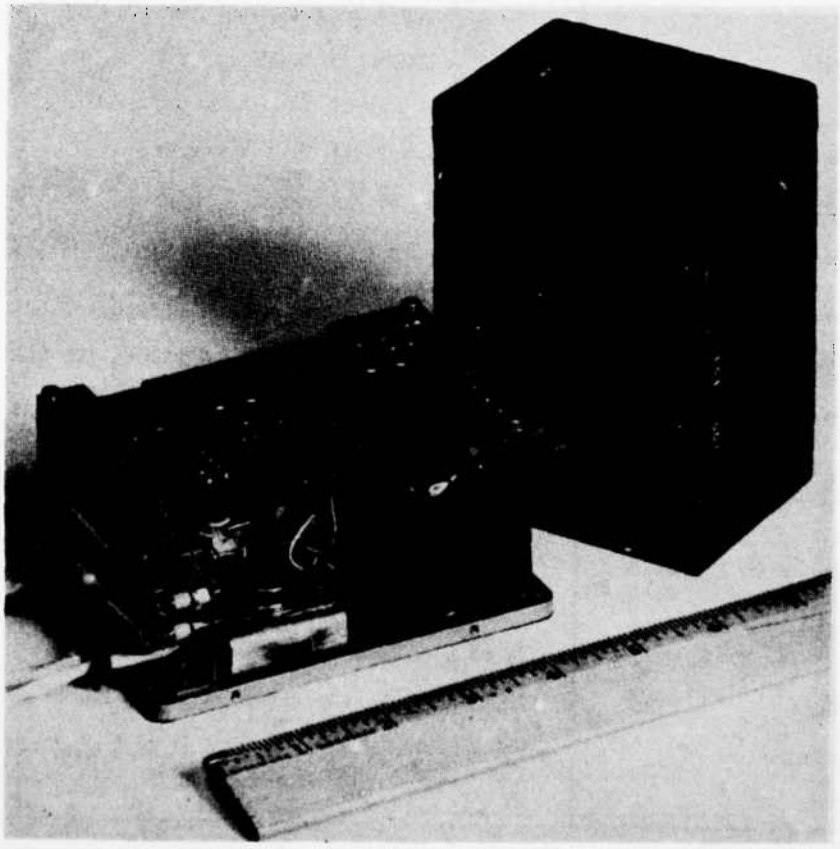


Figure A-13. Inverter

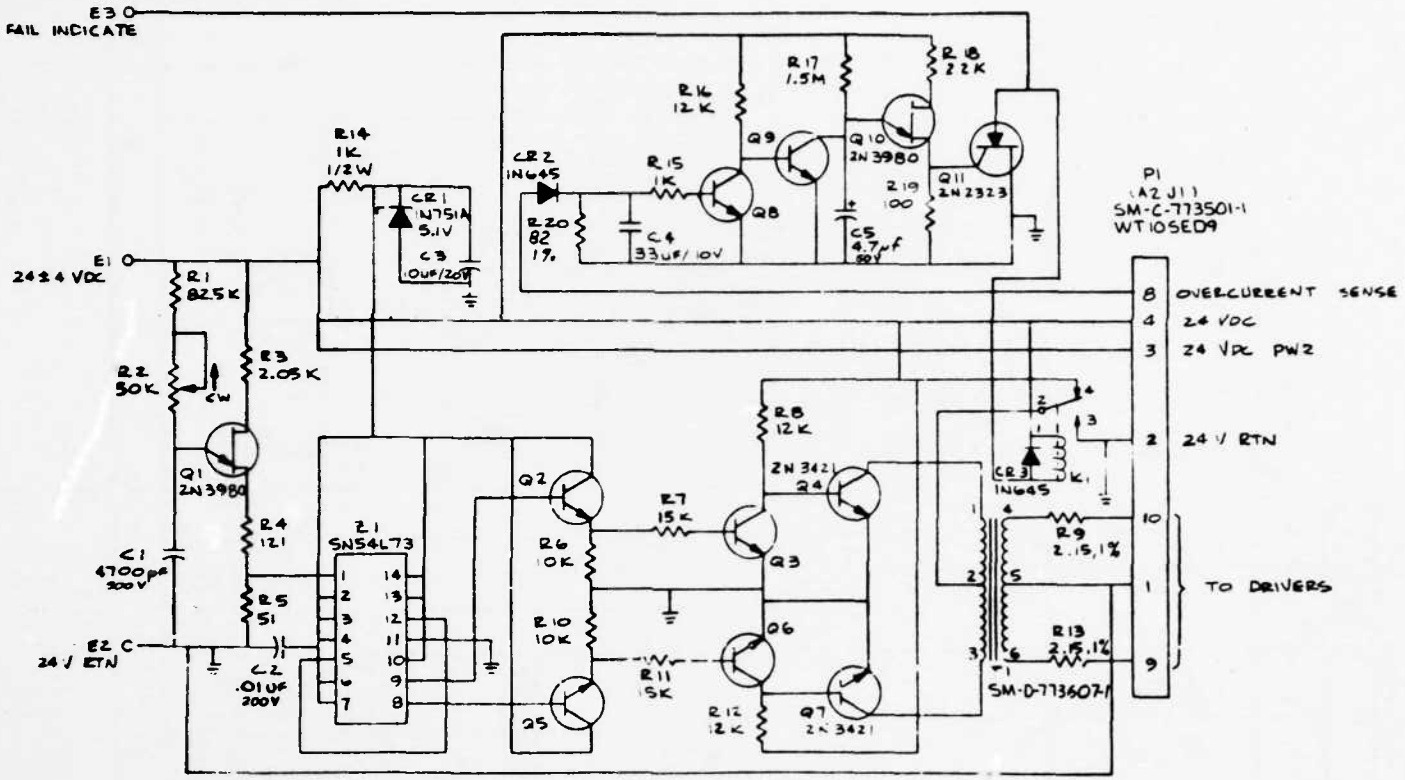


Figure A-14. Square Wave Generator Schematic

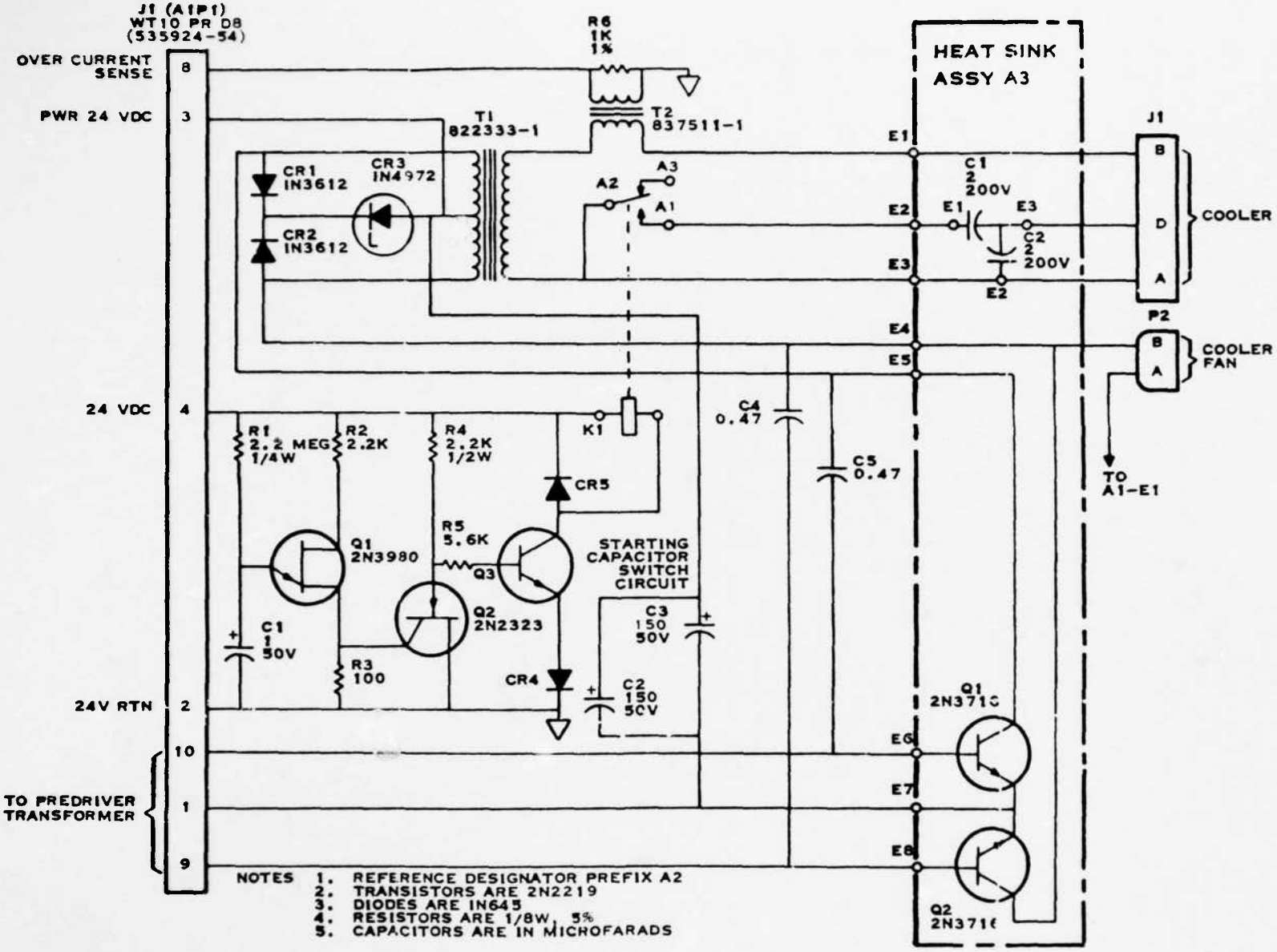


Figure A-15. Power Board Schematic

A.7.1 Square Wave Generator Board

Prime power is applied to A1 across a unijunction oscillator and a zener-diode 5-volt regulator. The oscillator provides an 800 pulse per second pulse train for ac generation. The narrow oscillator pulse is shaped into a symmetrical square wave by a J-K flip-flop which alternately turns on the buffer transistors Q2 and Q5. Transistor pairs Q3-Q6 and Q4-Q7 supply the necessary power gain to drive the predriver transformer T1. The output of T1 is an approximate 3.1 volts peak-to-peak, 400 Hz square wave. Also included on this board is the overload protection circuit comprised of semiconductors Q9 through Q11. In operation, C4 acts as a positive peak detector for the current sense signal at P1-8. When the overcurrent sense attains sufficient level (approximately 4 volts) to hold Q8 on and Q9 off, capacitor C5 begins to charge positive until Q10 fires turning Q11 on. When this happens relay K1 energizes, removing power from the predriver transformer, thus cutting off the 115 Vac, 400 Hz supply. This condition will remain until the overload has been corrected and prime power has been cycled off and on.

A.7.2 24-Volt Power Board

Prime power (24 $\pm$4 Vdc) comes into A2 from A1 on pins 3 and 4. The unijunction Q1 and the silicon controlled rectifier Q2 act as a one-shot device controlled by prime power turn-on. The initial output at R5 is high-level. This turns Q3 on, supplying ground to K1 and thus energizing the relay. This places the phase shifting capacitors C1 and C2 located on the heat sink across the cooler motor at turn-on. When the one-shot device changes state, Q3 is turned off, thus deenergizing relay K1 and removing the heat sink mounted capacitor C1 from the circuit.

The driver transistors Q1 and Q2 are located on the heat sink. They receive the 3.1 Vac, 400 Hz signal from the predriver and convert this signal to 24 Vac, 400 Hz at the primary of the driver transformer T1. The output of this transformer is 115 Vac, 400 Hz for the cooler motor.

Transformer T2 is located in one output line of transformer T1. This acts as a very low impedance in the line which senses the current drain. The output of T2 is the overcurrent sense applied to board A1.

Cooler and inverter module characteristics are shown in Table A-IX.

TABLE A-IX

Cooler and Inverter Characteristics

Parameter	Description
Input Voltage	24 ±4 Vdc
Output Voltage	115 ±19V, 400 Hz square wave primary phase with capacitor-shifted secondary phase
Nominal Operating Power	65W input at 50W output
Nominal Input Current	3.3 ±0.4A

A.8 Mechanical Scanner

Figure 3.3-1 indicates the overall size and weight of the mechanical scanner, and Figures 3.3-14 and A-6 show the module photographically. The scanner is supplied with a pigtailed connector for system electrical interconnect to power and control circuitry.

Three functions of the scanner are driven by electronic controls. These are the mirror scan rate, mirror angular travel, and interlace gimbal travel. Each function has a corresponding mechanical adjustment; for instance, the scanner assembly is supplied with interchangeable mirror

return springs of nominal 30 and 60 Hz ratings. Selection is a system-dependent choice based on performance evaluation. The spring mounts also allow for adjustment for different scan mirror angular travels. This can be calibrated by mechanical or electro-optical test methods, before locking the return springs into position.

Interlace axis travel is accomplished by the two solenoids. Each solenoid plunger assembly incorporates an interlace travel stop with a screw-thread adjustment. The electro-optical requirement for interlace axis excursion can be interpreted as a precise linear displacement at some radius to the axis. This displacement can then be achieved by adjusting the limit stops before locking the threads in position.

Typical characteristics and specifications for the mechanical scanner module are summarized in Table A-X.

TABLE A-X

Mechanical Scanner Characteristics

Characteriatics	Typical Meaaured Values	Specification
Interlace Ratio	2:1	2:1
Scan Frequency (Hz)	30, 42.5, 60	20 to 62
Scan Direction	Bidirectional	Bidirectional
Power: Watta at 60 Hz Watts at 30 Hz	7.3 4.0	$\leq$7.5 $\leq$4.0
Scan Efficiency Percent at 60 Hz, acan angle 10 degreea Percent at 30 Hz, scan angle 10 degreea	75 80	$\leq$70
Azimuth Jitter (mrad)	0.15	$\geq$0.75
Elevation Jitter Percent of Vertical Display Elevation	8	$\leq$10, $\geq$-10
Phaae Shift Lens Movement	0.002	
Azimuth Travel (degrees)	5, 7.5, 10	$\leq$10 maximum

A.8.1 Scanner Modulation Transfer

Scanner modulation transfer performance is listed in Table A-XI in terms of detector limiting spatial frequency, f_{co}. These MTFs will be used to compute system MTF.

TABLE A-XI

Scanner Modulation Transfer
(Typical Measured Data)

Scanner Frequency (Hz)	Spatial Frequency (f/f_{co})	Modulation Transfer Vertical	Horizontal
30	0.5	0.968	0.977
	1.0	0.820	0.900
60	0.5	0.960	0.960
	1.0	0.834	0.850

The scanner optical performance is tested by measuring the modulation transfer of the scanning mirror while the scanner is operating. The test setup for MTF measurement, diagrammed in Figure A-16, consists of a source of collimated visible light, four mirrors aligned to direct the beam to both sides of the scan mirror, an imaging lens, and a photmultiplier with associated electronics. The four-mirror alignment ensures invariance of the image position at the detector through all scan and interlace mirror positions. As the scanner operates, the quality of the imaged spot at the photomultiplier is analyzed to determine the MTF. The aperture stop of the test setup is within the imaaing optics; therefore, the aperture-dependent diffraction contribution to the MTF degradation is due solely to the test setup. This and any geometric wavefront error produced by the setup are determined by replacing the scanner with a diffraction-limited flat mirror

of the same thickness as the scanner and measuring the MTF. All MTFs measured with the scanner mirror are then divided by this number to normalize the setup MTF. The resultant figure represents a modulation transfer affected only by wavefront errors from the scanner mirror.

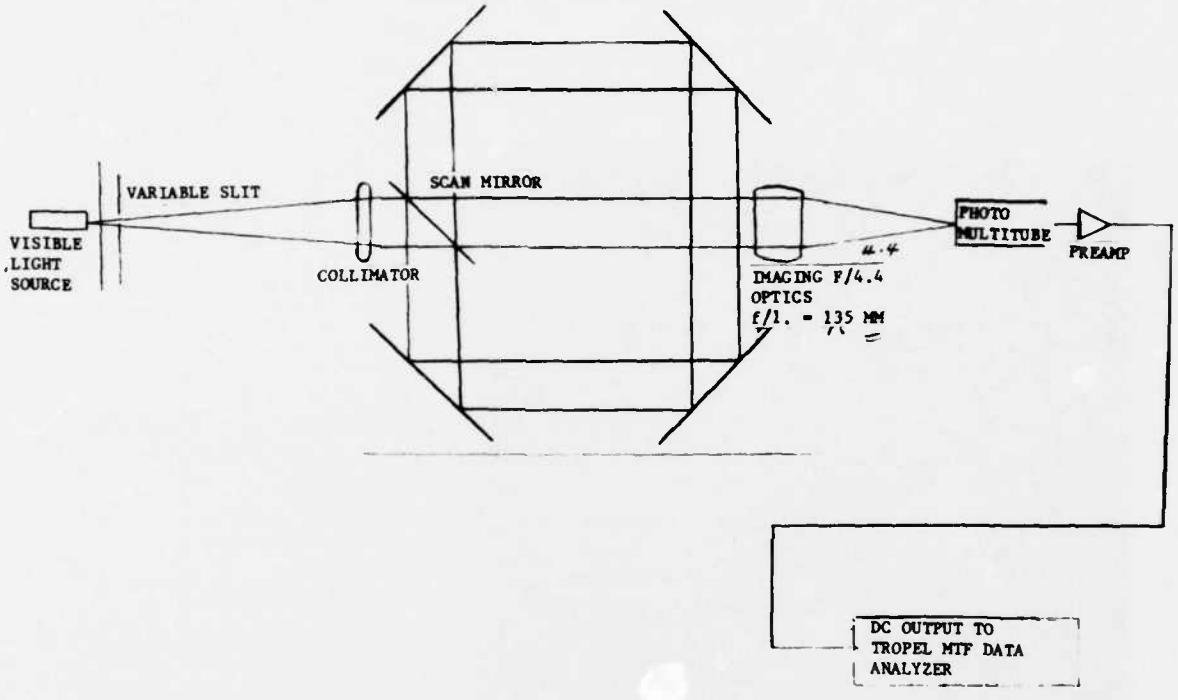


Figure A-16. Modulation Transfer Function Test Setup

The test setup averages the MTF over 2 degrees of mirror movement, while each field point is imaged by a separate scan mirror position for the system application. The difference between the cutoff positions for the test configuration and the system application produces slightly pessimistic MTF values. These values should be used as a worst-case system degradation factor, representing the combination of wavefront errors from both sides of the scanner at images near the optical axis $\pm$ 2 degrees of mirror motion.

A.9 Cooler

A.9.1 Principles of Operation

The cooler module (Figure A-17) is a miniature, closed-cycle refrigerator that operates on a thermodynamic cycle known as the Stirling cycle. The refrigerator extracts heat from the IR detector array to keep the operating temperature at approximately 80°K.

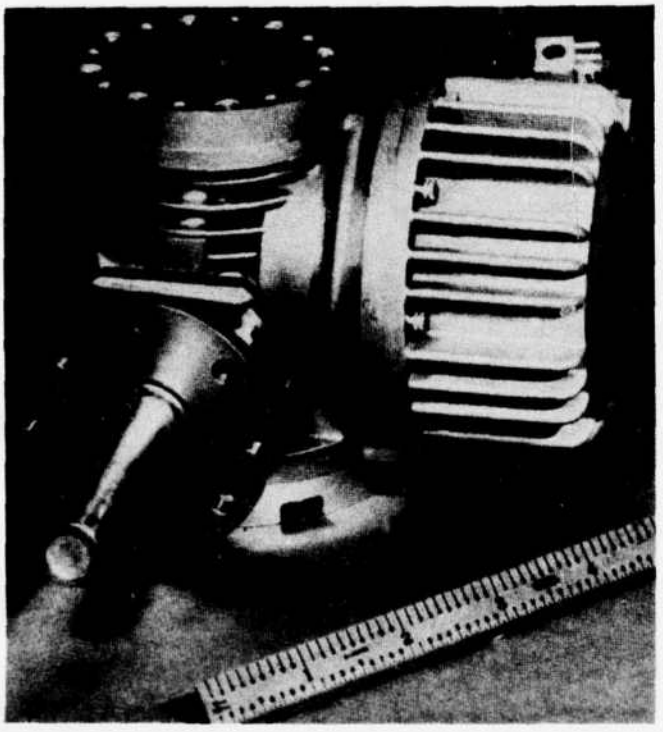


Figure A-17. Stirling Cycle Cooler

The Stirling-cycle refrigerator produces cold by the isentropic expansion of gaseous helium. In a closed cycle, the helium is alternately compressed in a compression space at ambient temperature and expanded to the required low temperature in an expansion space. The gas reciprocates between the compression and expansion spaces through a regenerator, which serves as a heat exchanger and heat sink for the incoming and returning gas flow.

The Stirling cycle can be described in terms of two isothermal (constant temperature) and two isochronic (constant volume) processes as shown in Figure A-18. In this figure, the compression piston, regenerator, and expansion piston are represented schematically and the contribution to the cycle pressure and volume curve is shown for each of the four processes. The cycle may be described in terms of these four processes as follows:

1. 1→2: Beginning with the expansion volume at its minimum and the compression space at its maximum, the compression piston moves to the left, compressing the gas in the compression space. As the gas is compressed, heat is removed from the cylinder walls so that the process is isothermal.
2. 2→3: Both the compression and expansion pistons move to the left, transferring the gas isobarically through the regenerator. During the transfer, the gas is cooled by the regenerator mass, which stores the heat contained in the gas, thus allowing it to enter the expansion space at the approximate temperature of that space.
3. 3→4: The expansion piston moves to the left, expanding the gas in the expansion space. As the gas is expanded, heat is absorbed from the thermal load (the detector elements) so that the process is isothermal.
4. 4→1: Both the compression and expansion pistons move to the right, transferring the gas isochronically through the regenerator from the expansion space back to the compression space. During the transfer, the gas is warmed by the stored heat in the regenerator, thus allowing the gas to enter the compression space at the approximate temperature of that space.

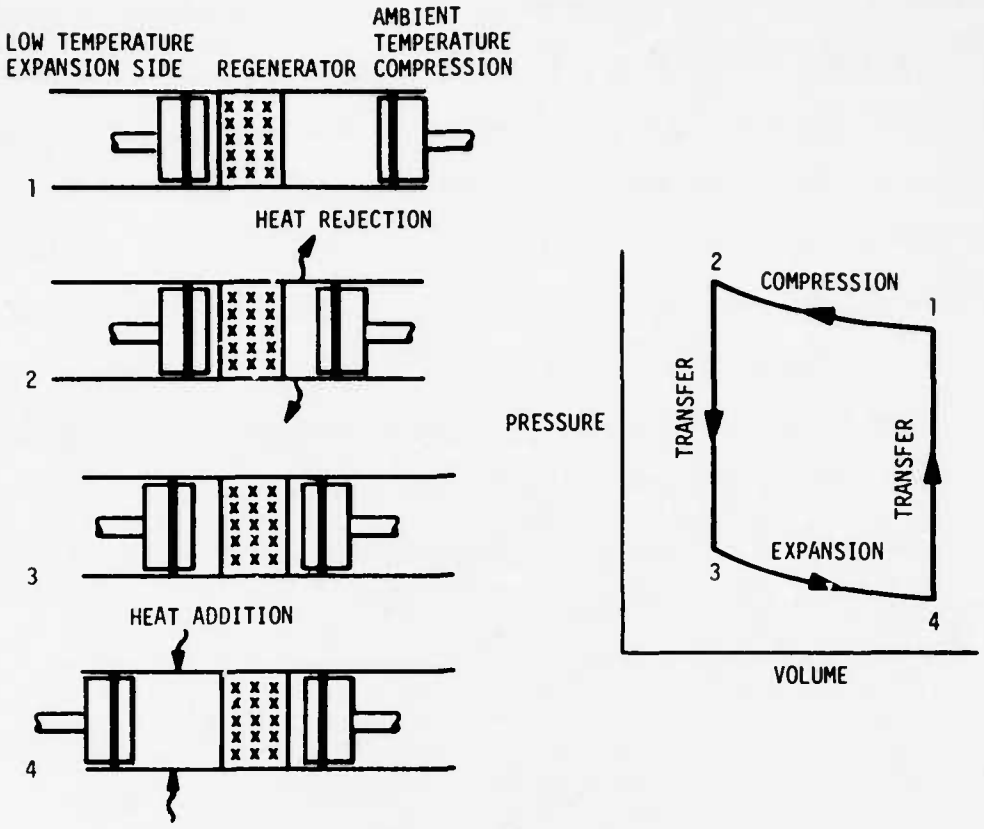


Figure A-18. Stirling-Cycle Refrigeration Process

The thermodynamic processes and schematic representations discussed above can be related to the actual cooler module hardware by referring to Figure A-19, which shows the cooler-detector/dewar assembly, and Figure A-20, which shows a detailed cross section of the cooler module. The necessary compression and expansion of the gas are accomplished by an out-of-phase motion of two pistons, thus eliminating the need for valves. The pistons are driven by an eccentric drive mechanism that is powered by an electric motor. The heat from the compression process is removed by fins attached to the housing and/or conduction through the compression head to a mounting bracket. Heat is added to the expansion space by conduction from the detector elements to the end of a glass stem assembly that has a thermal

conduction path through a nickel-copper bellows to the expansion volume. The detector elements and the glass stem assembly are contained in an evacuated dewar to minimize convection heat losses.

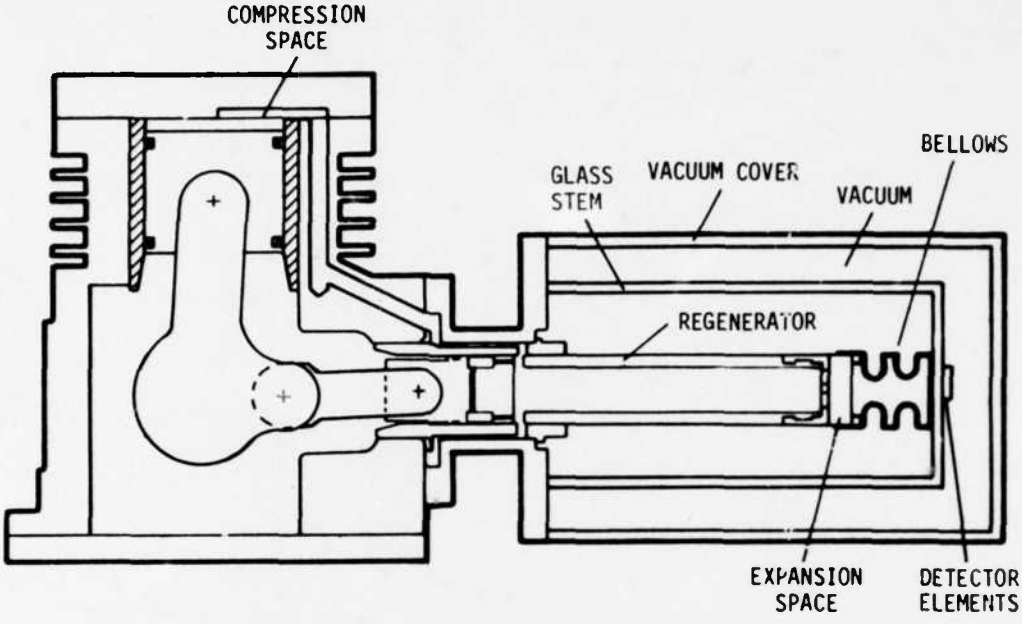


Figure A-19. Cooler - Detector/Dewar Assembly

A.9.2 Technical Description

A cross-section of the cooler showing the internal configuration (except for the motor) is shown in Figure A-20. The drive mechanism, motor, and compression piston are contained in a housing consisting of three castings and a cylinder head. Helium, which serves as the working fluid, is sealed within the housing. The compression piston and the regnerator/displacer are driven by an eccentric drive mechanism that is gear-linked to an electric motor. The regenerator/displacer is contained within the cold finger assembly, and the cold finger is thermally linked to the detector by means of a bellows which mounts over the end of the cold finger. Additional descriptions of some of these design details are contained in the following paragraphs.

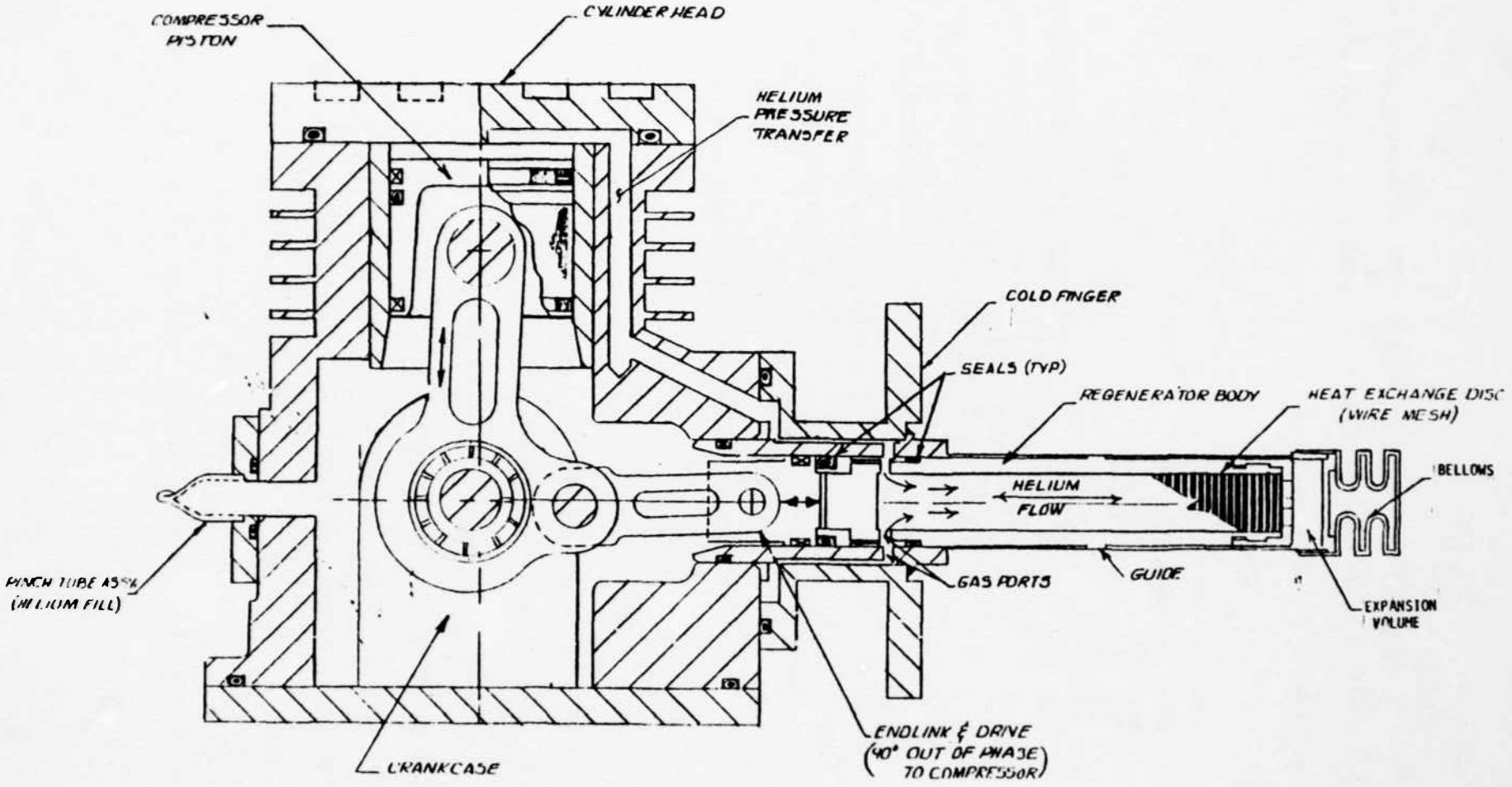


Figure A-20. Cooler Internal Configuration

A.9.2.1 Housing

The module housing consists of a machined aluminum cylinder head and three aluminum castings: cooler housing, motor housing, and base drive. The cylinder head, motor housing, and base drive are mounted to the cooler housing by means of bolts into helicoil inserts in the cooler housing. Helium flows from the compression space to the cold finger through a passage hole drilled in the cooler housing. The mounting flanges for the drive mechanism are an integral part of the base drive casting. All castings must be of high quality from a dense, pure aluminum alloy such as A356 because they form part of a helium pressure vessel. Any voids or defects will make the castings permeable to high pressure helium and result in a loss of helium pressure and thus in cooler performance. Since all aluminum castings are porous to some extent, impregnation or some other sealing process is required to prevent helium leakage via material porosity.

A.9.2.2 Working Fluid

A high purity grade (99.995 percent or better) helium at a pressure of 205 psia is used as the cooler working fluid. The cooler must be vacuum-baked, purged, and then back-filled with the working fluid to ensure that it is not contaminated with moisture, particulate matter, or other gases. Any of the contaminants can clog the regenerator screens and result in a significant reduction in cooler performance. Since helium is difficult to contain in a pressurized vessel and the cooler performance is a strong function of working fluid pressure, the castings and seals used to contain the working fluid must be carefully designed, fabricated, and assembled to ensure satisfactory cooler performance after long storage periods.

A.9.2.3 Seals

The common module cooler employs six static face seals and three internal dynamic seals. The static face seals are used at the following interfaces: main housing/cylinder head, main housing/base drive, main housing/motor housing, main housing/cold finger assembly, main housing/pinch-off tube assembly, and motor housing/electrical adapter. After assembly and pressurization, final sealing of the working fluid within the cooler is accomplished by a cold weld (pinch-off) of the copper tube on the pinch-off assembly. There is one dynamic seal on the compression piston and two dynamic seals on the seal sleeve, one on either side of the regenerator gas inlet port.

An indium wire seal of the configuration shown in Figure A-20 is employed for all of the static face seals. This sealing method is accomplished by laying 0.003 inch diameter indium wire with approximately 1/16-inch overlap into a gland whose design includes both a flash area and a preload gap to maintain pressure on the indium over a wide temperature range. Use of this indium wire seal offers the advantage of using a single wire size for all face seals while eliminating the problem of pressure loss due to material permeability, which is inherent in all standard elastomeric O-ring seal designs. Common module coolers have typically demonstrated leakage rates on the order of 1×10^{-8} std cm^3/s or less, a value that is one to two orders of magnitude below that which can be obtained with elastomeric O-rings.

The general configuration of the dynamic seals is shown in Figure A-20. The design combines a U-shaped cover with a one-piece stainless steel spring to provide uniform loading and high resilience over a wide

temperature range. The cover of the compression seal is fabricated from Fluocoloy K, a filled teflon material, and the regenerator seal covers are fabricated from molybdenum disulfide-filled teflon. On one unit that underwent reliability testing at Martin Marietta, such seals exhibited no failures in over 2000 hours of operation in a cyclic high- and low-temperature environment with periodic vibration exposure.

A.9.2.4 Drive Mechanism

The compressor and regenerator/displacer are motor driven through a single reduction gear set to an eccentric shaft. Two cranks, set at a 90-degree orientation on the eccentric shaft, provide the motion required to generate a 90-degree phase difference between the volume variations in the compression and expansion spaces. The imbalance inherent in this type of reciprocating device is the major contributor to vibration and acoustical noise output of the cooler. The bearings used in the drive mechanism must be lubricated with a material that has oxidative and thermal stability, is chemically inert, and has low volatility to minimize the impurities introduced into the working fluid by the lubricant.

A.9.2.5 Motor

The motor used to power the drive assembly described above is a brushless ac electric motor that rotates at approximately 5400 r/min. The reduction gear has a ratio of 3.5:1 so that the drive mechanism rotates at 1540 r/min. The motor operates on 117 volt, 400 Hz, single-phase power and provides a full load torque of 5 oz-in. The motor is mounted by shrink-fitting into the motor housing.

A.9.2.6 Cold Finger Assembly

The cold finger assembly is constructed of three stainless steel parts: flange, tube, and cap. The flange provides mounting surfaces for attaching the cold finger assembly to the crankcase housing and for attaching the detector/dewar assembly to the cold finger. The inside of the tube serves as the cylinder wall for the reciprocating regenerator (or displacer) piston. The wall of the tube must be as thin as structural considerations permit to minimize conduction heat losses along the length of the tube. The cap seals the cold finger tube and is the wall separating the cold expansion volumes from the thermal load.

A.9.2.7 Regenerator/Displacer

An exploded view of the regenerator/displacer assembly is shown in Figure A-21. The end link connects the assembly to the drive mechanism. The guide, fabricated of Rulon, centers the assembly in the cold finger tube. The seal sleeve serves as a mounting cylinder for the regenerator seals and is the connecting link between the end link and the regenerator body. The regenerator body houses the discs and is fabricated from a laminated epoxy material. This material has the required properties of low thermal expansion and low thermal conductivity. The guide on the body is machined as an integral part of the body. The body is filled with approximately 600 stainless steel wire mesh screen discs. The material from which the discs are fabricated is 0.001-inch diameter S5 303 wire mesh having 200 openings per inch. The stack of discs has the required properties of large surface area, large heat capacity, and low longitudinal thermal conductivity to serve as a heat exchanger and a heat sink. The stack of discs removes heat from the

working fluid during the transfer from the compression to the expansion space. The discs are held in place by a cap that is epoxied onto a shoulder in the regenerator body. Due to the large number of parts, small passage ports for the working fluid, and close tolerances in the regenerator assembly, the regenerator should be one of the first areas examined in the event of a cooler failure.

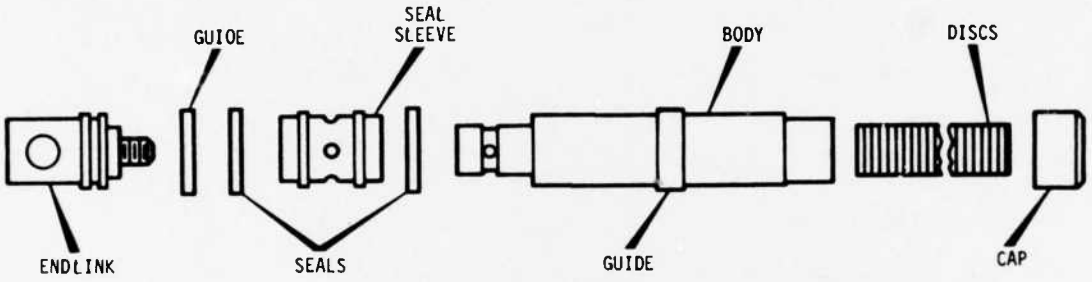


Figure A-21. Regenerator/Displacer Assembly

A.9.2.8 Bellows

The bellows is a lamination of nickel and copper that provides a thermal conduction path between the cold finger cap and the glass stem assembly to which the detector elements are mounted. The bellows fits over the end of the finger, and conductive grease is used at the interface to reduce the thermal resistance between the two. When the cold finger is inserted into the detector/dewar assembly, the bellows is depressed and spring loaded against the inside of the glass stem assembly, thus providing a thermal path betweer the cold expansion volume and the detector elements.

A.9.3 Specifications

The detailed specifications for the cooler are contained in the development specification B2-28A050108A. The physical and performance characteristics are summarized in Table A-XII for an ambient temperature of 23 ±2°C.

(Figure A-22 and Table A-XIII provide information associated with Table A-XII).

TABLE A-XII

Cooler Characteristics

Characteristic	Value
Weight	3.7 pounds maximum
Envelope Dimensions	3.6 x 4.0 x 6.9 inches
Cooling Capacity	Figure A-22
Cooldown Time*	10 minutes max for 100K detector temperature
	15 minutes max for 80K detector temperature
Input Power	50 watts
Acoustical Noise	Table A-XIII
Service Life	10 years minimum
Storage Life with no Helium Refill	2 years minimum
Vibration Output	$\leq$2 pounds @ 26$\pm$4 Hz along the compressor piston, motor, or cold finger axis

*For a 600 Joule thermal mass equivalent and a 0.200 watt thermal load comprised of the sum of the dewar radiative loading and the Joule heating of a resistive heating element.

A.9.4 Representative Test Data

Table A-XIV shows room temperature data for seven delivered common module coolers and low- and high-temperature data for one delivered cooler. The data shown includes cooldown times, minimum temperature, temperature with 1 watt electrical load, net cooling capacity, and input power at 77°K. All data were taken with a 600 Joule thermal mass cold station. All load values shown are resistive heating values. No corrections are included for dewar radiation losses and no radiation shielding was employed.

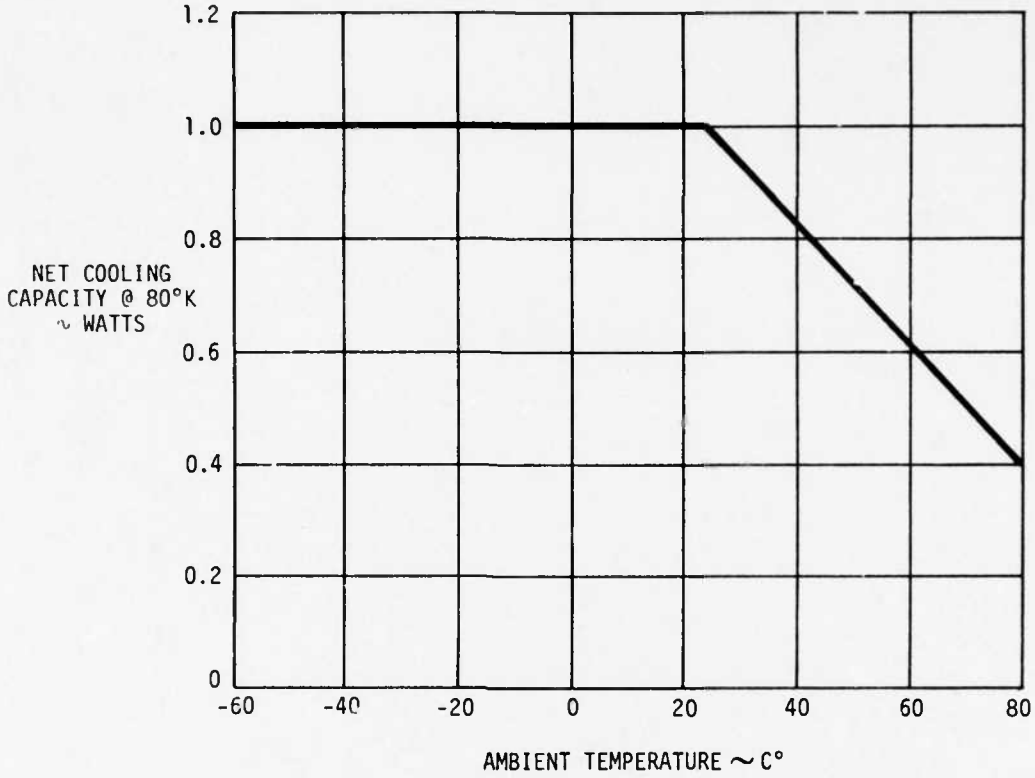


Figure A-22. Cooling Capacity

TABLE A-XIII

Maximum Cooler Noise at 25 Feet

Center Frequency (Hz)	Octave band (Hz)	Maximum Sound Pressure Level (dB) Reference 0.0002 μbar
125	87 to 175	40
250	175 to 350	39
500	350 to 700	34
1000	700 to 1400	32
2000	1400 to 2800	35
4000	2800 to 5600	36
8000	5600 to 11,200	34

TABLE A-XIV.

Representative Cooling Capacity and Input Power Data for Common Module Cooler

	Ambient Temperature (°F)	Cooldown Time to 100°K (min)	Cooldown Time to 77°K (min)	Minimum Temperature (°K)	Temperature with 1W load (°K)	Input Power at 77°K (W)	Cooling Capacity at 77°K (W)*
6 Different Coolers	79.8	6.2	7.6	46.0	73.8	45	1.14
	73.7	6.1	7.6	47.2	73.3	44	1.17
	74.4	5.8	7.2	50.1	74.8	48	1.11
	77.1	6.4	7.8	45.5	75.8	46	1.08
	73.8	7.4	9.2	47.4	77.5	42	1.00
	72.7	6.5	8.0	45.6	73.3	43	1.16
1 Cooler	-65	5.6	7.0	38.9	69.0	45	1.28
	129	7.8	10.2	56.7	75.4 (0.68 W)	46	0.75
	160	8.5	11.0	59.9	73.7 (0.50 W)	50	0.64

*Values shown are input power to load resistor. No correction made for dewar losses. No radiation shielding employed.

Vibration data for three delivered common module coolers are shown in Table A-XV. As indicated in the table, some of the data were generated by Martin Marietta and some by NVL. The procedure employed in generating the Martin Marietta data was with the cooler rigidly attached, using the mounting holes on the compressor head, to a test plate that suspended as a bifilar pendulum with a natural frequency of less than 2 Hz. The cooler was oriented so that the motor shaft was along the vertical axis. Three accelerometers were attached to the test plate using rubber mounting pads to filter high frequency noise. The accelerometer mounting frequency was less than 100 Hz, and the accelerometers were mounted so as to sense accelerations along the motor, piston, and cold finger axes. The measured acceleration values were then used to calculate the amplitude of the vibrational forces along each of the three axes.

TABLE A-XV

Representative Vibration Output Data for Common Module Cooler*

Frequency (Hz)	Cooler Serial No.	Data Generated By	Axis	Vibrational Force (lb)
26	001	MMC	Piston	1.23
26	001	MMC	Cold finger	1.36
26	007	MMC	Piston	1.13
26	007	MMC	Cold finger	1.10
27	001	NVL	Motor	0.685
27	001	NVL	Piston	1.639
27	001	NVL	Cold finger	1.317
27	003	NVL	Motor	0.568
27	003	NVL	Piston	1.904
27	003	NVL	Cold finger	1.429

*All data shown is for cooler with spur gears.

A.10 Infrared Imager

The IR optical imager (Figure A-23) is the module that forms an image of the scene on the linear detector array. In a system application, collimated light from the system afocal assembly is directed by the mechanical scanner along the optical axis and into the aperture of this module.

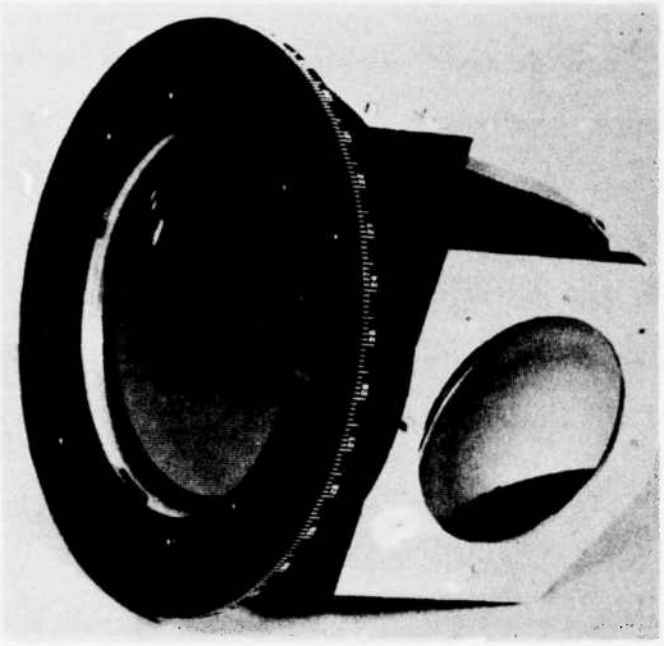


Figure A-23. IR Optical Imager

The module consists of three lens elements and a folding mirror. The two elements forward of the folding mirror, one TI-1173 IR transmitting material and one germanium, are movable. This capability is used to adjust focus position during assembly. The third element of germanium following the folding mirror is fixed. The mechanical layout of the IR imager is shown in Figure A-24.

Because the TI-1173 IR optical material was not available at the time from the prime source, redesign was required to permit the use of an alternate material. Since it was considered desirable to meet the performance of

the original design where it exceeded the specification, a goal was set to achieve a design that required only the respecification of the optical elements. A design was achieved that required no changes to the mechanical housing and spacers.

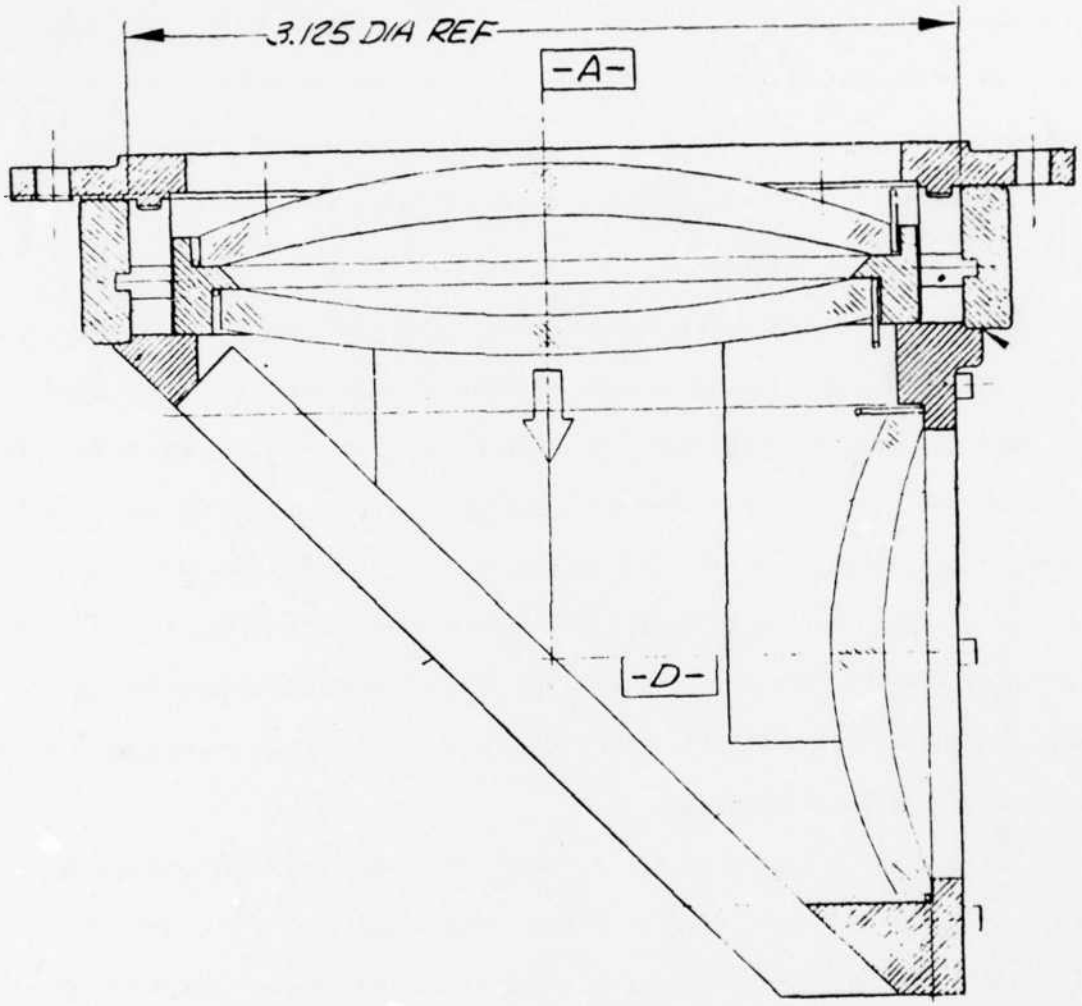


Figure A-24. Mechanical Layout of IR Imager, PN SM-D-804143

Infrared material, modulation transfer configuration, focus adjustment, distortion, and optical transmission are discussed in the following paragraphs.

A.10.1 Infrared Material

Selection of new IR lens material was based on its similarity to the TI-1173 optical material and the average absorption over the spectral bandpass of 7.5 to 11.75 μm. Polycrystalline ZnSe was chosen. It has an index 2.407 at 10 μm compared with 2.6036 for the TI-1173. The abbe value or relative dispersion of ZnSe (for the 8 to 12 μm band) is 58.6 compared with 107.6 for TI-1173. Average absorption coefficient for the ZnSe is 0.004 cm^{-1} as compared with 0.173 cm^{-1} for TI-1173.

A.10.2 Modulation Transfer

The modulation transfer functions for the axial and 5 mm off-axis field points using a radial target orientation with the images at f/1.8 are shown in Figures A-25 and A-26. The focal plane was chosen to provide the best MTF over a 10 mm format. Included in the figures are the specification requirements for MTF, the design values, and the spread of measured values on eight imagers to date. The measured values compare to the design values within the error of measurement. At the higher frequencies the measured values fell slightly below the design values but remain well above the specification requirement.

The imager is tested at f/1.8. Typical system applications use the imagers in the range of f/1.8 to f/2.5. When used with the common module mechanical scanner the imager is limited to f/1.69 as the scan mirror becomes the aperture stop for the imager. The design f number of the imager alone is f/1.07.

A.10.3 Configuration

The mechanical constraints imposed by requiring the redesigned optical elements to mount in the originally designed housing were not serious.

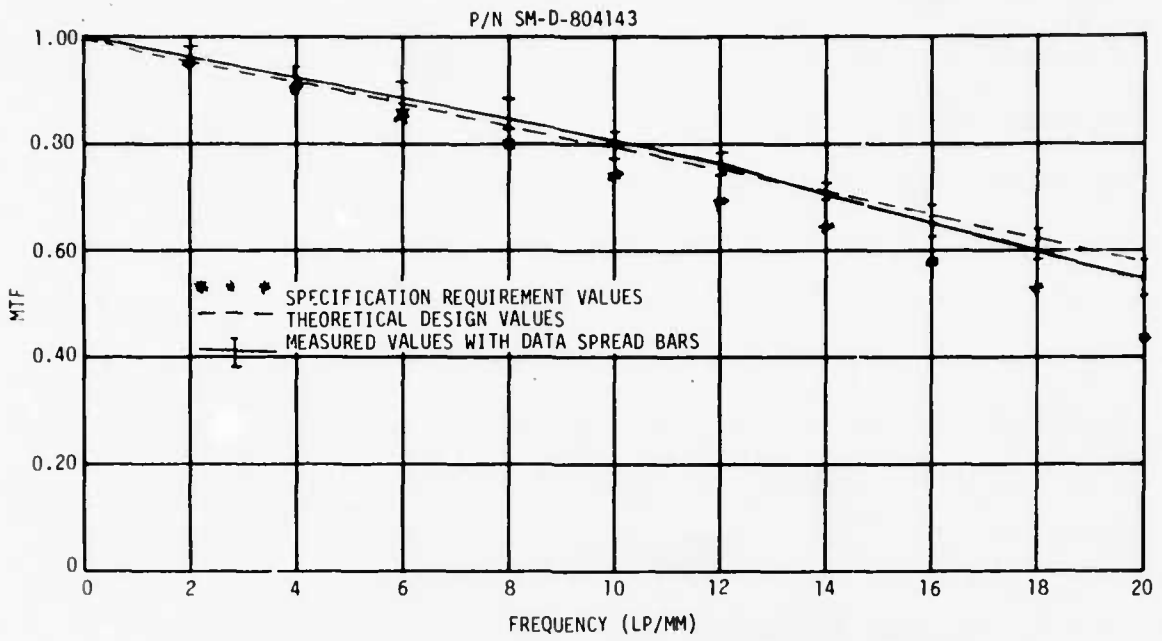


Figure A-25. Large IR Imager Modulation Transfer On-Axis

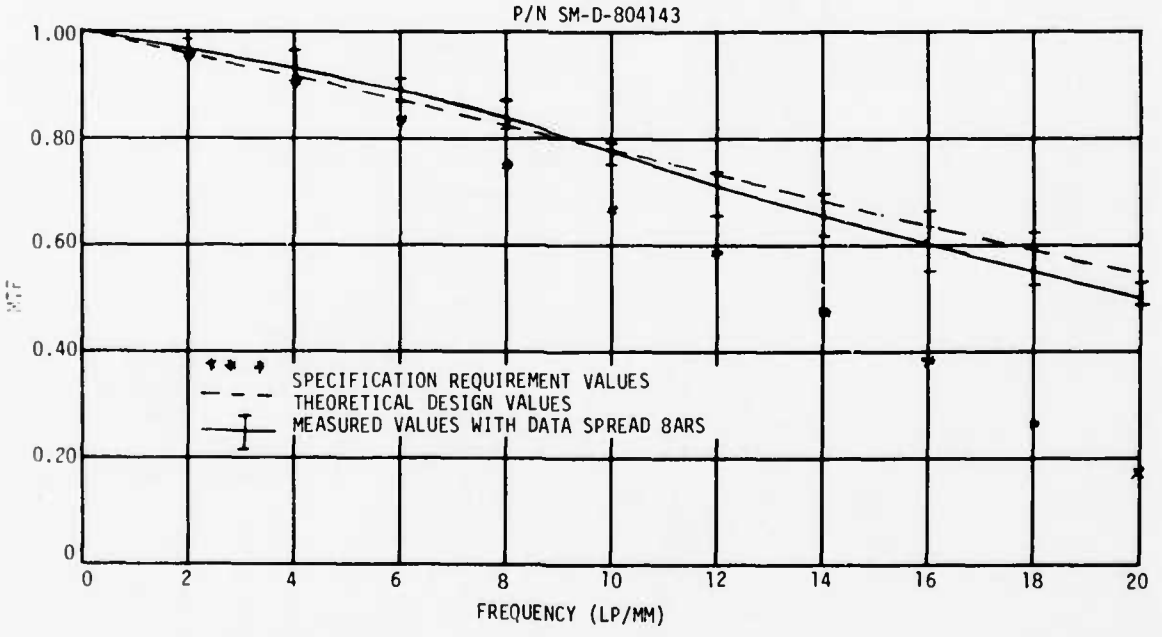


Figure A-26. Large IR Imager Modulation Transfer Half Field (5mm)

Figure A-27 shows the mechanical constraints of the original and redesigned systems, and Table A-XVI shows the basic lens data. The distance from the flange of the second element to the flange of the rear element is identical, 2.953 inches. This is adjustable and provides focus from a minimum of 2.883 +0.024, -0.034 inches to a maximum of 3.043 +0.024, -0.014 inches. These rather large tolerances are due to the peculiar method used to tolerance the mechanical design. The flange distance between the first two elements is 0.081 ±0.020 inch. The flange focal distance specified in the development specification B2-28A050104 (28 June 1974, 17.86 ± 0.25 mm) is to be checked without the dewar window.

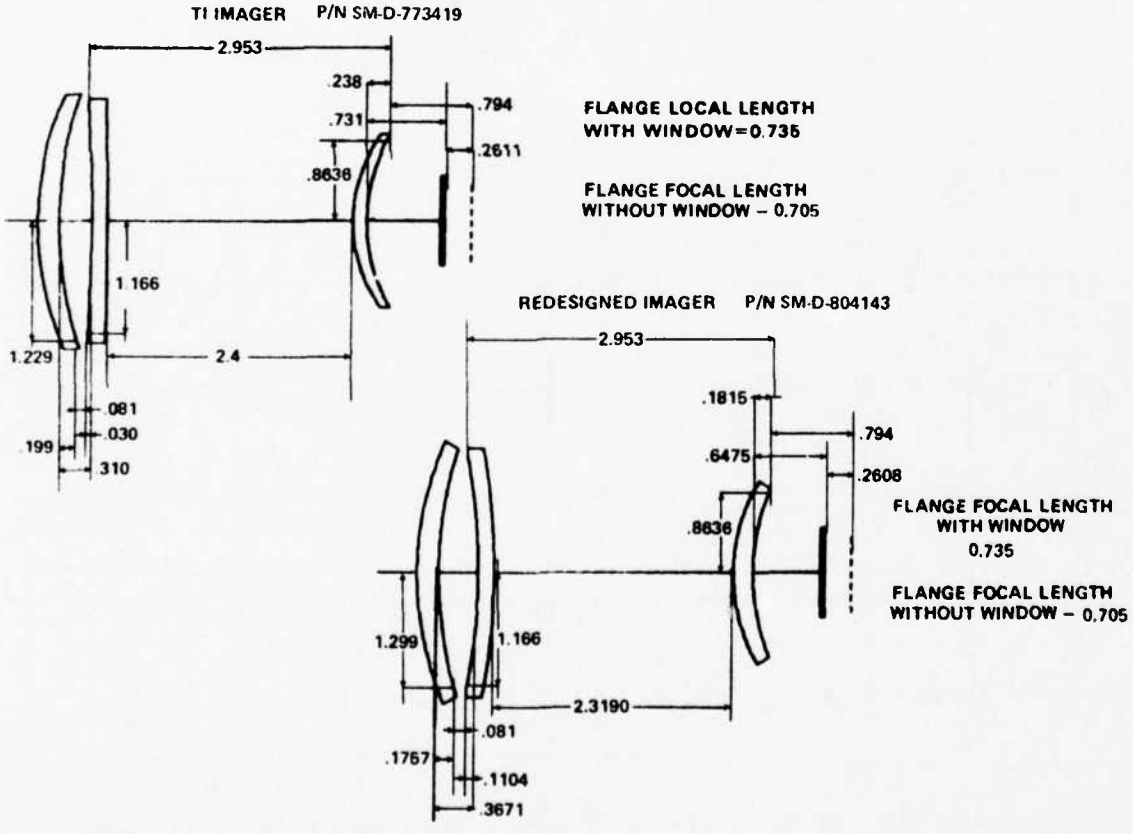


Figure A-27. Mechanical Housing Constraints for the IR Imager

TABLE A-XVI

Infrared Imager Lens Data

Surface	RD	TH	MEDIUM	RN	CA
0	0.0	0.100000D 13	AIR		
1	0.0	2.400000	AIR		
2	3.396500	0.200000	MATL - GERM	4.003074	2.5
3	4.384500	0.367000	AIR		2.4
4	-6.214000	0.150000	ZnSe	2.407000	2.28
5	-7.132300	2.319000	AIR		2.30
6	1.782000	0.192000	MATL - GERM	4.003074	1.70
7	2.144700	0.674500	AIR		1.60
8	0.0	0.040000	MATL - GERM	4.003074	
9	0.0	3.059197	AIR		
10	0.0	-2.798414	AIR		
11	0.0	0.0	AIR		
EFL	BF	F/NBR	LENGTH	GIH	
2.6628	0.2608	1.66	6.3425	0.3934	

RD = Radius

TH = Thickness

RN = Index of refraction

CA = Clear aperture

EFL = Effective focal length

BF = Back focal length

LENGTH = Length from aperture stop surface to dewar window

GIH = Gaussian image height

When the detector module is installed in the system, the window will increase the flange focus distance to 18.67 mm as shown in Figure 3 of the development specification. The effects on performance of the window are negligible, permitting testing without the window.

A.10.4 Focus Adjustment

The 15 Nov 76 (REVA) development specification requires the flange focal distance to be adjustable 0.47 mm on either side of the nominal flange focal length value. The adjustment will be afforded by the rotation of the focusing ring gear.

Constraining the redesigned optical elements to the original housing and meeting the specified flange focal distance controlled the power ratio of the movable front elements so that the focus requirements were exceeded in the original design. Figure A-28 shows the calculated range focus characteristics of the original and AnSe designs.

Table A-XVII lists the focus adjustment data on the original (TI, P/N SM-D-77349) ZnSe redesign (P/N SM-D-804143). Given are total linear motion of the front groups and the total image shift this motion affords. Image shift per degree rotation of the focus ring is given along with thermal shift characteristics of the two designs. The focus adjustment requirement affords a minimum of $\pm$9.47 mm focus adjustment while typical total focus adjustment measured on the ZnSe designed imagers is more on the order of $\pm$1.2 mm. A thermal focus shift has been measured on one imager and the data reduced to 3.1×10^{-4} in/°C compared to a design value of 2.56×10^{-4} in/°C. A larger test sample is required to achieve a more reliable value of the thermal focus shift of the large imager. The $\pm$0.47 mm required focus adjustment affords design temperature compensation for a ΔT of $\pm$72.2°C or range focus down to 9 meters.

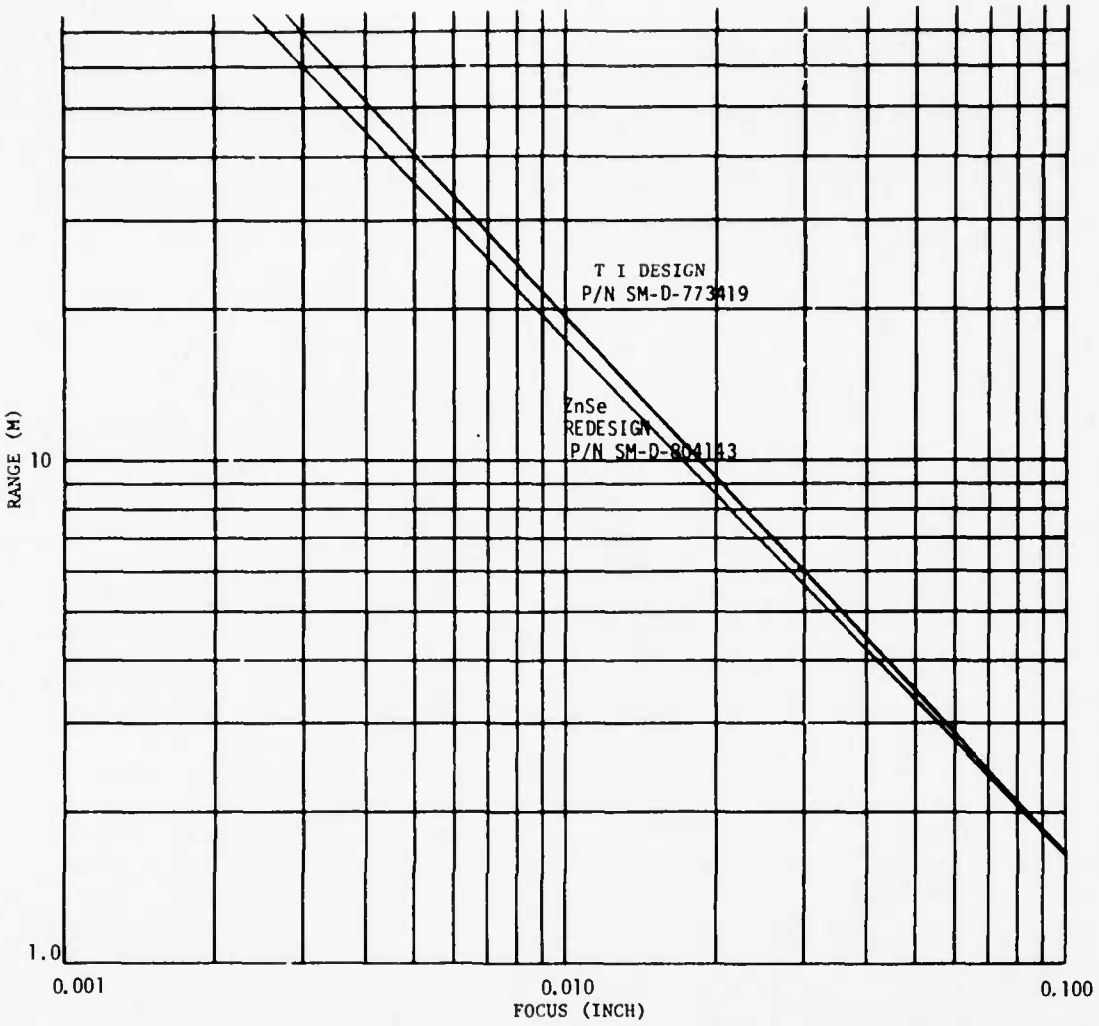


Figure A-28. Range Focus Characteristic - Common Module Imager

TABLE A-XVII

Focus Adjustments - IR Imager

	P/N SM-D-773419 TI Design	P/N SM-D-804143 ZnSe Redesign
Allowable Linear Lens Shift	+0.070 inch -0.090 inch	+0.070 inch -0.090 inch
Linear Lens Shift: Image Shift Ratio	3.66	3.38
Image Shift/Degree Rotation Focus Ring	0.00019 inch	0.00020 inch
Total Available Image Shift	0.04371 inch	0.04734 inch
Range Focus	See Figure A-28	See Figure A-28
ΔFocus/ΔT	2.64×10^{-4} inch/°C (Calculated)	2.56×10^{-4} inch/°C (Calculated)

A.10.5 Module Specifications

Table A-XVIII* compares the performance of the ZnSe and TI 1173 IR imagers to the development specification. Given are design values and measured values for the ZnSe redesign.

TABLE A-XVIII

Specifications for TI-1173 and ZnSe IR Imager

Development Specification B2-28A050104A	Specification	P/N SM-D-773419 TI-1173 Design	P/N SM-D-804143	
			ZnSe Redesign	ZnSe Measured
Focal Length (mm)	67.8 ± 0.7	68.280	67.635	67.65
Distortion (percent)	±4.0	-2.16	-1.12	-0.9
f/Number	1.19	1.08	1.07	Tested at 1.1
Relative Illumination	0.60	0.90	0.90	0.85
Flange Focal Length, No Window (mm)	17.86 ± 0.25	17.90	17.88	17.78
FOV (degrees) (20 mm Format)	8.44	8.52	8.52	8.52
Transmission	0.85	0.85	0.85	0.89
Deviation from 90 Degrees (degrees)	0.5	<0.5	<0.5	0.4
Modulation Transfer				
10 lp/mm				
On-Axis	0.74	0.78	0.78	0.76
5mm Off-Axis (T/R)	0.66	0.78/0.75	0.78/0.77	0.78/0.74
20 lp/mm				
On-Axis	0.44	0.63	0.57	0.53
5mm Off-Axis (T/R)	0.18	0.54/0.44	0.55/0.52	0.56/0.53
Weight, ±0.05 pounds	1.15		1.12	

A.10.6 Distortion

A distortion analysis was completed on the IR imager and the results given in Figure A-29. Measured distortion was -0.9 percent compared with a design value of -1.12 percent.

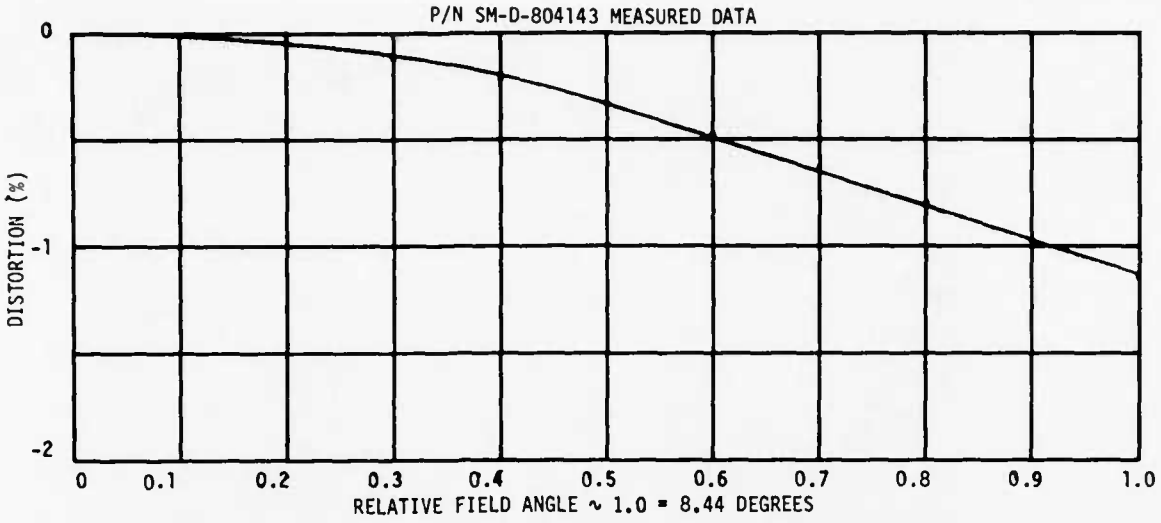


Figure A-29. Large IR Image Linear Distortion

A.11 Visual Collimator

The visual collimator module (Figure A-30) collects light from the LED array and projects collimated light onto the mechanical scanner. The collimator consists of eight optical elements and a folding mirror in a modified petzval configuration (Figure A-31). Six elements are cemented into three doublets and one of the two single elements is included in the LED array as the window. The petzval configuration provides minimum secondary color at relatively low f number at the expense of field curvature. To minimize the image degradation at off-axis field points, the window of the LED array is curved for negative power. This compensation succeeds at small field angles. Since the field required is 16.8 degrees, satisfactory results were achieved. The effect of the residual higher-order image errors on the system performance in the scan direction was minimized by adjusting the power of the LED array window to place the sagittal focal plane at the LED array. The tangential errors have little effect on the system performance perpendicular to the scan direction because of the LED overlap (Figure 3.2-4).

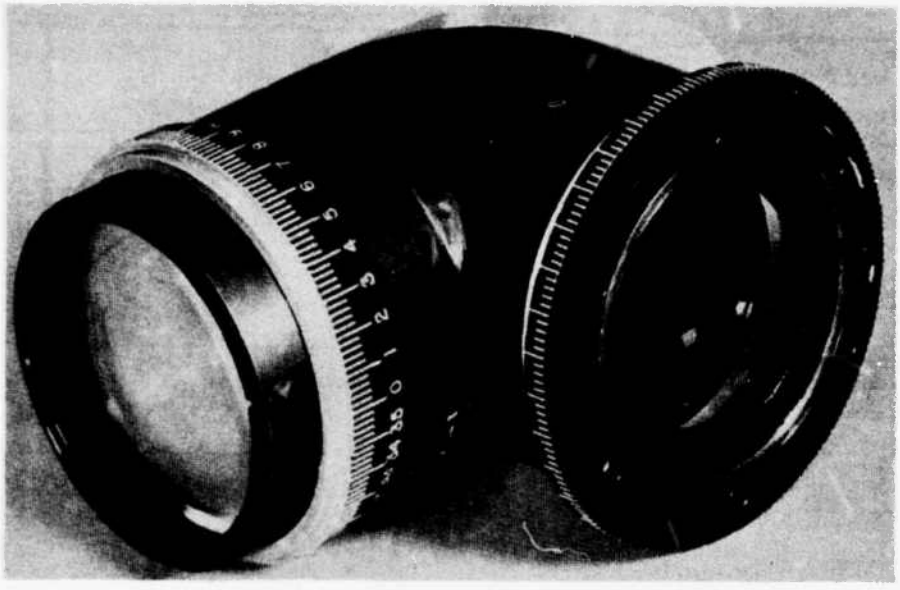


Figure A-30. Visual Collimator

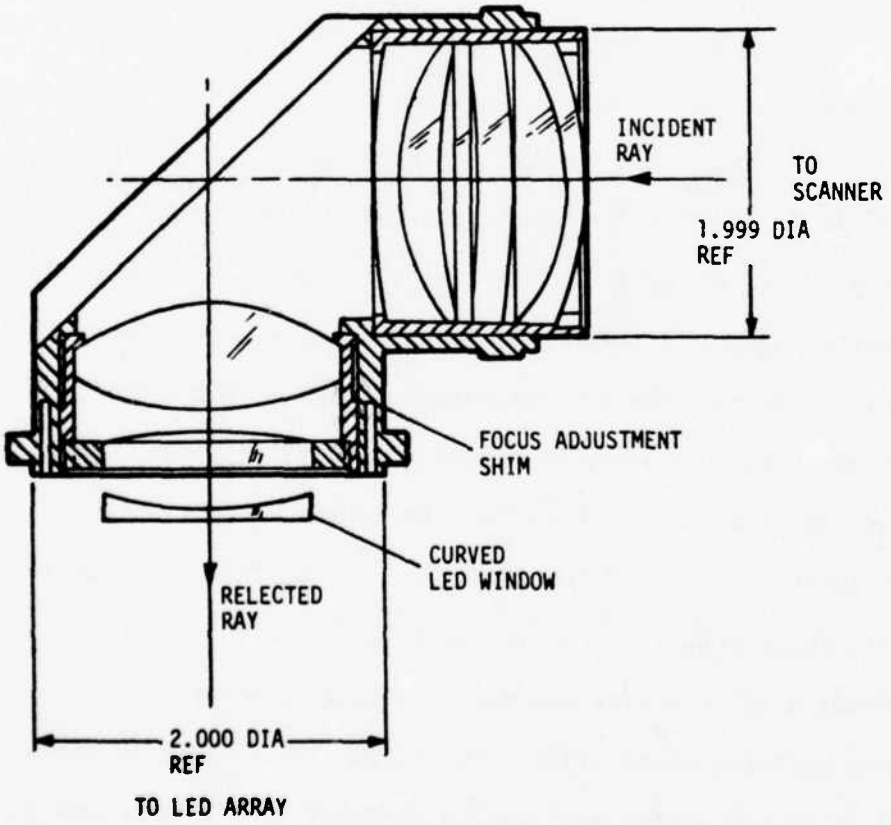


Figure A-31. Visual Collimator Mechanical Layout

As shown in Figures A-32 and A-33, computed design MTF and actual measured MTF for five visual collimators both exceed development specification (B2-28A050105A) values. At a spatial frequency of 10 line pairs per millimeter, a modulation transfer on-axis of 0.96 compares favorably with the specification figure of 0.93. The modulation transfer measured in the sagittal plane at half-field and at 10 lp/mm shows a value of 0.94, again exceeding the specified value of 0.86.

The visual collimator module is achromatized at 0.45 and 0.65. However, ray traces show that the chromatic errors between 0.63 and 0.69 μm do not affect performance. Wavelengths emitted from the array are specified in the LED development specification (B2-28A050103) to be 0.66 +0.050 -0.100 μm, while the visual collimator is required to meet performance between 0.63 and 0.69 μm. This margin will permit the half-power bandpass of the emitted wavelengths to be 0.300 μm and a frequency shift with time and temperature of -0.050 to +0.100 μm.

The optical prescription of the visual collimator common module is summarized in Figure A-34. This figure is an output of the optical design program ACCOS V developed and maintained by Scientific Calculations, Inc. Clear apertures and lens parameters have been included along with the lens formula. The collimator, although plotted in a straight line form, contains a folding mirror between the two groups of optical elements.

The aperture of the visual collimator allows an f number of 1.69, with the aperture stop being the first element of the collimator. This design is faster than the specified requirement of 1.718. However, in most system applications the ray bundle is limited by an aperture stop separated from the collimator by the scanner module, effectively stopping the collimator down

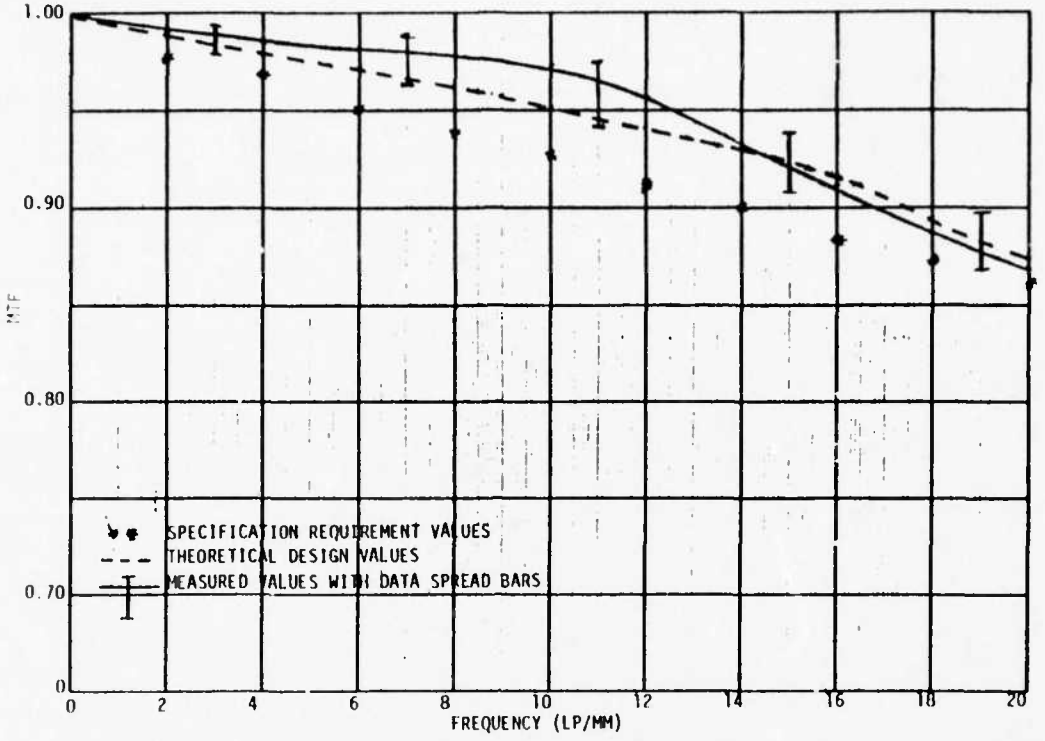


Figure A-32. Visual Collimator Modulation Transfer On-Axis

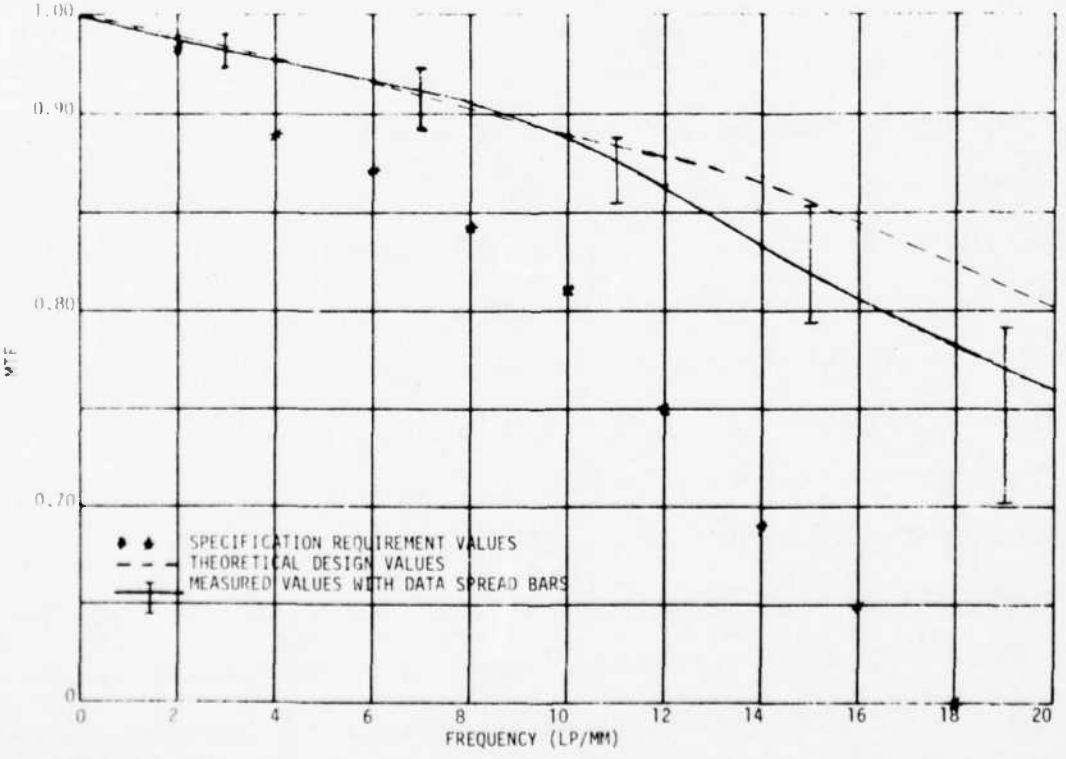
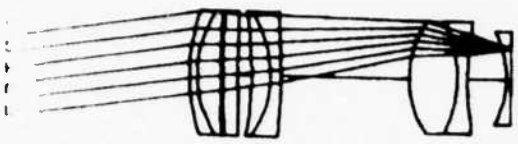


Figure A-33. Visual Collimator Modulation Transfer Half Field (5 MM)



FOCAL LENGTH 2.67 IN.
FLANGE FOCAL LENGTH 11.3±0.05 MM
FIELD VERTICAL 17.1 DEG.
FORMAT 20 MM
TRANSMISSION 0.92 (0.63 TO 0.69 M)
APERTURE STOP 1.23 IN. AT 2.36 IN.
F/NUMBER 2.2

BASIC LENS DATA

SURF	RD	TH	MEDIUM	RN	CAs
0	0 0	0 100000D+13	AIR		
1	0 0	2 360000	AIR		
2	2 318000	0 100000	SCHOTT F2	1.614806	1.58
3	1 405000	0 319000	SCHOTT SK2	1 603986	1.58
4	136 750000	0 020000	AIR		1.58
5	17 155000	0 200000	SCHOTT SK2	1.603988	1.58
6	26 532000	0 181000	AIR		1.57
7	-4 415000	0 250000	SCHOTT SK2	1.603986	1.57
8	-1 330700	0 138000	SCHOTT F2	1.614806	1 58
9	-7 636000	1 710000	AIR		1 58
10	1 199300	0 643000	SCHOTT SK2	1.603986	1.42
11	-1 587000	0 140000	SCHOTT F2	1.614806	1.42
12	3 458600	0.520000	AIR		1.18
13	-1 200000	0 060000	SCHOTT F2	1.614806	1.18
14	0 0	-4 523389	AIR		1.18
15	0 0	4 578288	AIR		
16	0 0	0 0	AIR		

Figure A-34. Visible Collimator Optical Prescription

to f/2.2. Such a configuration simplifies the design of the relay optics used to refocus the collimated LED light. Approximately 17 percent vignetting will occur in the vertical field with this aperture stop located 2.36 inches beyond the collimator when using the full complement of IR channels.

Comparison of specified parameter values to typical values is outlined in Table A-XIX, which lists measured values as typical. In all cases, measured data were verified by computed data. Data were measured and computed with the collimator as described in the optical prescription using spectral weighting of 1.0 from 0.63 to 0.69 μm. Note that transmittance and relative

illumination parameters critical to the system performance exceed their requirements by significant amounts.

TABLE A-XIX

Collimator Characteristics

Parameter	Specification B2-28A050105A	Typical Measured Values
Effective Focal Length	67.8 ± 0.7	67.89 ± 0.5
f/Number	<1.718	1.69
Distortion (percent)	±4 max	-1.1
Modulation Transfer f/2.2 stop 60 mm Forward, 23°C		
10 lp/mm		
Axial	0.93	0.96
5mm Off-Axis	0.86	0.94
20 lp/mm		
Axial	0.86	0.87
5mm Off-Axis	0.58	0.82
Stray Light Veiling Glare (percent)	5	2
Relative Illumination f/2.2 stop 60mm Forward, Full Field	>0.60	0.83
Flange Focal Length (mm)	11.91 ± 0.25	Adjust Shim
FOV, 20mm Format (degrees)	8.4	8.4
Transmission (percent) λ, 0.63 to 0.69 μm	>0.85	0.92
Deviation (degrees)	<0.5	Adjust Mirror

A.12 Light Emitting Diode Array

The LED array (Figure A-35) consists of 180 elements. The GaAsP elements are composed of a single crystal compound of gallium, arsenic, and phosphorous. The color of the emitted light (red, 6600Å) is obtained by controlling the concentration of phosphorous. The relationship of forward current to emitted light is nearly linear. Because this intensity may vary from element to element for a given input current, a normalization resistor located within the module is placed in series with the LED driver. Empirical data indicate values of normalization resistors vary from 125

to 300 ohms for a typical array. These resistors are located within the array and cannot be changed. Typical characteristics of the LED array are given in Table A-XX, and array element dimensions are shown in Figure 3.2.4.

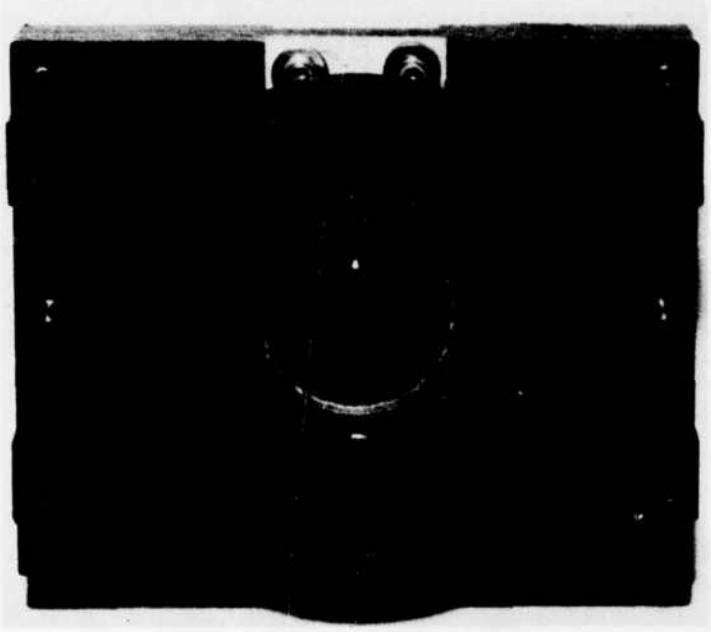


Figure A-35. Light Emitting Diode Array

TABLE A-XX

Light Emitting Diode Array Characteristics

Wavelength	6600 +50, -100 Å
Power Output (I_{in} = 2 through 15 mA)	0.94 μW/mA minimum
Forward Voltage* (Includes diode and series normalization resistor)	2.3 Vdc typical @ 5 mA
Current Rating	≥ 15 mA
Time Constant	≤ 0.3 μs

* The forward drop of the LED is approximately 1.6 Vdc for currents from 1 to 10 mA.

APPENDIX B

VIDEO ELECTRONICS NOISE ANALYSIS

B.1 General

The primary contributors to the total noise referenced at the input to the preamplifier are: 1) preamplifier, 2) preamplifier regulator, 3) preamplifier ripple, 4) detector, 5) detector bias regulator, 6) detector ripple, and 7) postamplifier ripple. This analysis considers only these sources of noise. Other sources of noise (such as background) can be included as required. The resultant noise from all sources, Ent, is shown in Figure B-1.

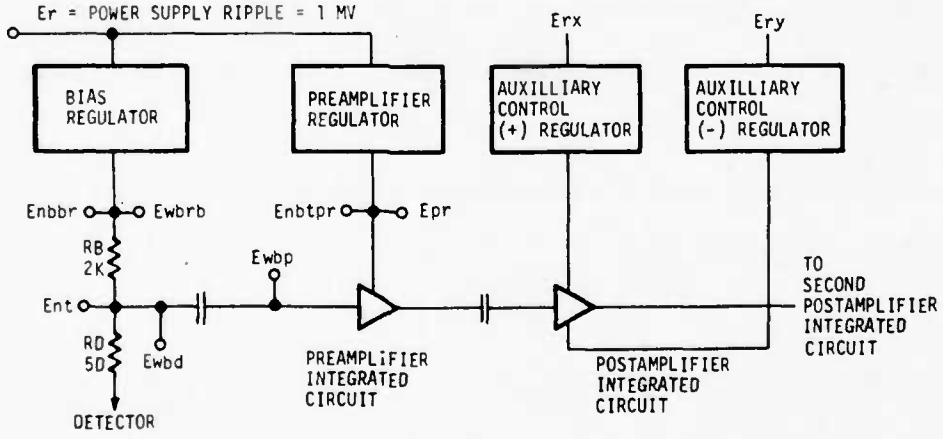


Figure B-1. Noise Analysis

The procedure used to perform the noise analysis is described below. The equivalent noise bandwidth for the video electronics is determined in section B.2. This bandwidth is different for the detector and preamplifier sources and neglects the effects of 1/f noise. The fact that the 1/f noise is negligible for all sources is proven in section B.3 using the electronics bandwidths determined in section B.2. The noise due to the preamplifier, preamplifier regulator, preamplifier ripple, detector, detector bias regulator, detector ripple, and postamplifier ripple are considered in sections B.4 through B.10. A noise summary is contained in section B.11.

B.2 System Noise Bandwidth Considerations

If the 1/f noise is considered negligible as proven in section B.3, then the total equivalent noise appearing at the input to the preamplifier is determined primarily by the upper cutoff frequency of the video electronics. The system bandwidth (which included all contributors) was determined in paragraph 3.4.1.2 to be from 7 Hz to 70 kHz with 18 dB/octave slopes for both the lower and upper rolloffs as shown in Figure 3.4-16. The noise analysis can be greatly simplified by assuming the three poles that determine the overall bandwidth to be identically located. This assumption is proven in the following sections to be valid without introducing a significant amount of error.

The expression for the noise bandwidth can be determined for any system by evaluating

$$fn = \frac{1}{Ao^2} \int_0^\infty A^2 (f) df$$

for a first-order system in which

$$A (f) = \frac{Ao}{\left[1 + \left(\frac{f}{fc}\right)^2\right]^{1/2}}$$

where

Ao = mid-band gain

fc = single pole location

$$A^2(f) = \frac{Ao^2 \cdot fc^2}{fc^2 + f^2} .$$

Therefore,

$$fn = \int_0^\infty \frac{fc^2 \cdot df}{fc^2 + f^2}$$

and, in general, for an nth-order system:

$$fn = fc^{2n} \int_0^\infty \frac{df}{(fc^2 + f^2)^n} .$$

Solving, $$fn = \frac{\pi fc}{2} \left[\frac{[2(n-1)]!}{4^{(n-1)} \cdot [(n-1)!]^2} \right] .$$

Letting f2 = total system upper 3 dB cutoff frequency, then

$$fc = \frac{f2}{(2^{1/n} - 1)^{1/2}}$$

and

$$fn = \frac{\pi(f2)}{2(2^{1/n} - 1)^{1/2}} \left[\frac{[2(n-1)]!}{4^{(n-1)} \cdot [(n-1)!]^2} \right] .$$

Solving the expression,

$$fn = \frac{\pi(f2)}{2} = 1.571(f2) \text{ for a first-order system}$$

$$fn = \frac{\pi(f2)}{2.574} = 1.22(f2) \text{ for a second-order system}$$

$$fn = \frac{3\pi(f2)}{8.16} = 1.16(f2) \text{ for a third-order system.}$$

This analysis demonstrates that, for a third-order system with identically located poles, the overall bandwidth is equal to 1.16 times the system upper 3 dB cutoff frequency. If two of the poles were identical and the third pole were moved to infinity, the error introduced would be only 6 percent for fn because this is the difference between a second- and third-order system and less than 3 percent for the total noise which is increased by the square root of the bandwidth.

The system detector and video electronics show a third-order rolloff with a 3 dB bandwidth of 70 kHz. The noise bandwidth is:

$$fn = 1.16(f2) = 1.16\ (70\ kHz) = 81.2\ kHz\ .$$

The fn determined for the complete video electronics is used for the following sources of detector associated noise: detector, detector bias regulator, and detector ripple. For the other sources of noise described in section B.1, the bandwidth is broader because the detector time constant does not contribute to the overall bandwidth; for example, the contribution from the preamplifier is not directly affected by the time constant of the detector. A computer run was made eliminating the frequency effects of the detector, and moving the upper 3 dB cutoff frequency to f2 = 80 kHz with a rolloff of 12 dB/octave (gain-squared rolloff of 24 dB/octave) as shown in Figure B-2. The resulting noise bandwidth for the preamplifier, preamplifier regulator, preamplifier ripple, and postamplifier ripple is:

$$fna = 1.22(f2)$$

$$fna = 1.22\ (80\ kHz) = 97.6\ kHz.$$

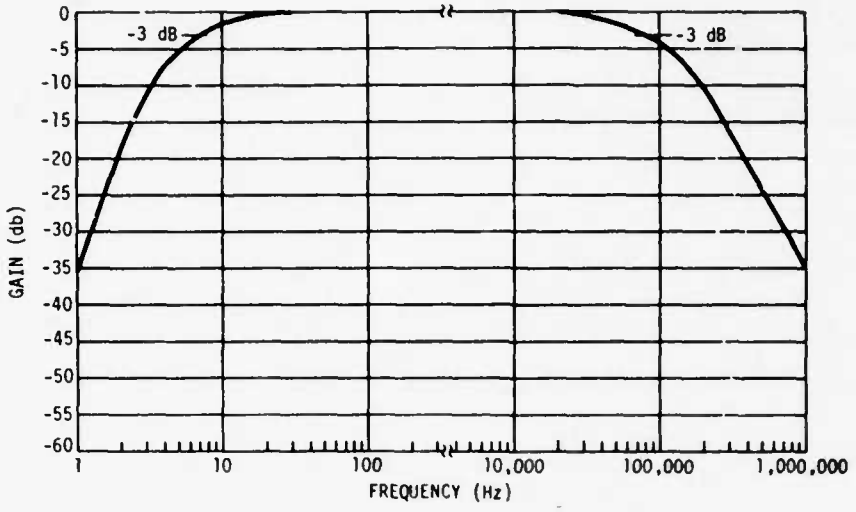


Figure B-2. Nominal Video Electronics Bandwidth Less the Detector-Associated Contributors

B.3 1/f Noise Consideration

This section demonstrates that the 1/f noise can be neglected for the primary noise contributors mentioned in section B.1. In particular, the 1/f noise can be neglected for the detector, the bias regulator, the preamplifier, and the preamplifier regulator for noise bandwidths in the range of 80 kHz.

For a first-order system, the following expressions are used to identify gain as a function of frequency for the low- and high-frequency responses, respectively:

$$A_L(f) = \frac{Ao}{[1 + (f1/f)^2]^{1/2}}$$

$$A_H(f) = \frac{Ao}{[1 + (f/f2)^2]^{1/2}} .$$

For f small, $A_L(f)$ becomes

$$A_L(f) = Ao\left(\frac{f}{f1}\right)$$

and for f large, $A_H(f)$ becomes

$$A_H(f) = Ao\left(\frac{f2}{f}\right).$$

Here f1 = the lower 3 dB cut-on frequency. These expressions can be altered to accommodate rolloffs of N1 and N2 d3/octave as shown in Figure B-3 by the dashed lines:

$$A_L^2(f) = Ao^2\left(\frac{f}{f1}\right) N1/6$$

$$A_H^2(f) = Ao^2\left(\frac{f2}{f}\right) N2/6 \quad .$$

N1 and N2 represent the gain-squared rolloff (i.e., a 6 dB/octave gain rolloff corresponds to a 12 dB/octave gain-squared rolloff). For the complete video electronics, N1 = N2 = 36 dB/octave.

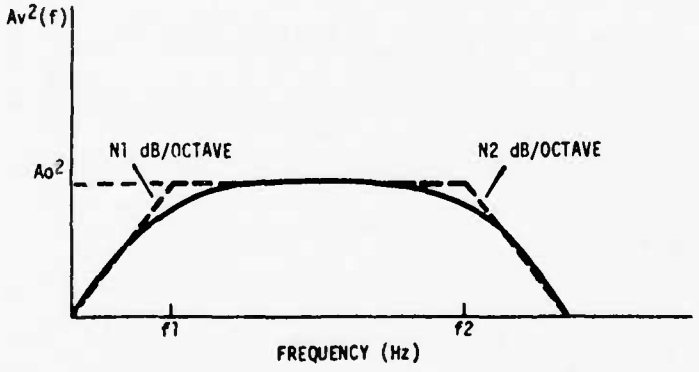


Figure B-3. Typical System Frequency Response

The 1/f noise spectral density for electronics devices is shown in Figure B-4. The equation that describes this curve is:

$$Enb^2(f) = Enbo^2\left[1 + \left(\frac{fB}{f}\right)^2\right]^{1/2}$$

and for f small

$$Enb^2(f) = Enbo^2 \left(\frac{fB}{f}\right)$$

where

Enbo = flat portion of the noise power spectrum ($nV/\sqrt{Hz}$)

fB = noise power spectrum 1/f break frequency.

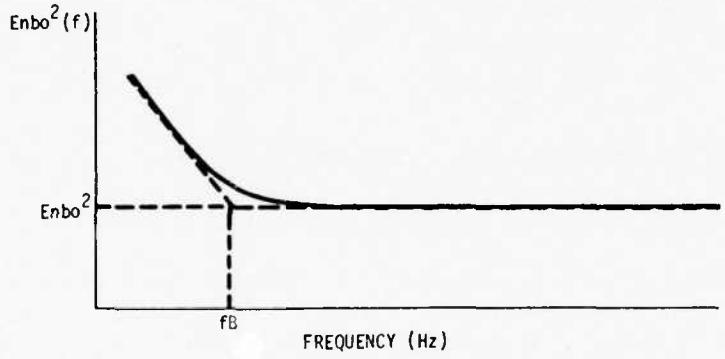


Figure B-4. Noise Spectral Density

The total noise can be found by integrating the product of the noise density function times the square of the system frequency response where Enwb = wideband noise level:

$$Enwb^2 = \frac{1}{Ao^2} \int_o^\infty Av^2 \, Enb^2(f) \, df$$

or

$$Enwb^2 \simeq \left[\int_o^{f1} Enbo^2 \left(\frac{fB}{f}\right)\left(\frac{f}{f1}\right)^{N1/6} df + \int_{f1}^{fB} Enbo^2 \frac{(fB)}{f} \, df \right.$$

$$\left. + \int_{fB}^{f2} Enbo^2 \, df + \int_{f2}^{\infty} Enbo^2 \left(\frac{f2}{f}\right)^{N2/6} \, df \right].$$

When evaluated, the approximate expression becomes:

$$Enwb^2 \simeq Enbo^2 \left[f2 \frac{(N2)}{N2-6} + fB \frac{(6 - N1)}{N1} + \log\left(\frac{fB}{f1}\right)\right].$$

For the video electronics, f1 = 7 Hz, f2 = 70 kHz, N1 = 36 dB/octave, N2 = 36 dB/octave, and fB = 1 kHz (the assumed knee for the noise power spectrum of any 1/f source). Solving,

$$Enwb^2 = Enbo^2 \left(70\ kHz \left(\frac{36}{30}\right) + 1\ kHz \left(\frac{-30}{36}\right) + \log\left(\frac{1000}{7}\right)\right)$$

$$Enwb^2 = Enbo^2\ (84\ kHz - 0.835\ kHz + 2.15).$$

Therefore, $Enwb^2 \approx Enbo^2 \left(\frac{f2 \cdot N2}{N2 - 6}\right) = 1.2\ Enbo^2$.

This expression demonstrates three important facts. First, the approximate expression yields results that indicate that the 1/f noise adds little to the overall noise for the 70 kHz, third-order system ($\sqrt{84\ kHz}$ - $\sqrt{83.165\ kHz}$ = > error $\leq$ 0.5 percent). Second, the error is even less for the second-order, 80 kHz, 3 dB cutoff frequency, f2 (for a third-order cutoff f2 of 25 kHz, error $\leq$ 1.7 percent). Third, this analysis demonstrates that the overall noise is limited primarily by f2 alone, which can be equated to the third-order expression derived in section B.2 in which fn = 1.16 (f2); from the approximation expressed by the wideband noise level equation fn = 1.2 (f2), and the error is less than 4 percent. If fB is moved to 5 kHz, the contribution of the 1/f noise causes an error in the overall approximation of less than 2.4 percent.

B.4 Preamplifier Noise

The preamplifier itself contributes two sources of noise. One is the white noise, Enbp, specified to be 1.5 nV/$\sqrt{Hz}$, while the other is 1/f noise specified to be 10 nV/$\sqrt{Hz}$ at 100 Hz. The 1.5 nV/$\sqrt{Hz}$ specification is a composite of preamplifier and regulator noise. The 1/f corresponds to an fB $\approx$ 4.5 kHz in Figure B-4, and its contribution can be neglected as described in section B.3. The preamplifier wideband noise can be calculated to be:

$$Ewbp = Enbp \sqrt{fna}$$

$$Ewbp = 1.5 \times 10^{-9} \sqrt{97.6\ kHz}$$

$$Ewbp = 0.469\ \mu V.$$

B.5 Preamplifier Regulator Noise

Although preamplifier regulator noise is included in the specified preamplifier noise, this analysis is included to demonstrate that regulator noise is negligible. The preamplifier regulator generates noise as a function of its biasing and feedback components. In reality, the preamplifier regulator itself is no more than an amplifier with feedback. It is designed to reject power supply ripple appearing at the preamplifier without introducing significant noise itself. Regulator noise, however, does appear at the input to the preamplifier, V_{cc} (Figure 3.4-1), because the regulator does not have infinite power supply rejection. Power supply rejection is defined as the ratio of the voltage change at the input due to a voltage change on the supply lines. Power supply ripple rejection in the module preamplifier regulator is a function of frequency as illustrated by empirical rejection data represented by curve B in Figure B-5. (The source of the preamplifier was loaded with 50 ohms.) A loss in rejection is seen to occur as a function of frequency. This loss in rejection also effectively results in greater regulator noise appearing at the input to the preamplifier because less regulator noise rejection is available when power supply ripple rejection decreases.

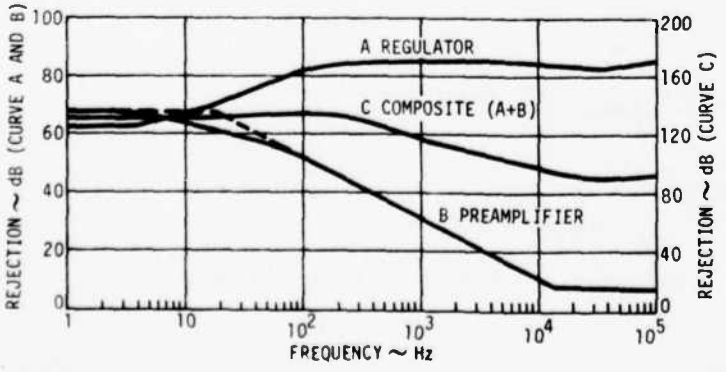


Figure B-5. Preamplifier and Preamplifier Regulator Power Supply Rejection (test data)

The noise of the preamplifier regulator can be determined by referring to Figure B-6. The three major contributors of noise are the zener diode ($Enbz^2$), R3 ($Enbr^2$), and the amplifier noise ($Enba^2$), which is primarily a function of the input stage (a 2N930 transistor whose noise characteristics are shown in Figure B-7). The 2N930 is biased at approximately 4 mA and yields an equivalent noise at the input of Enba of 6×10^{-9} $V/\sqrt{Hz}$. The 1/f noise for the regulator can be neglected as determined in section B.3 as its fB breakpoint is approximately 5 kHz for 4 mA of bias current. This approximation introduces about 3 percent error in the total noise output for the regulator.

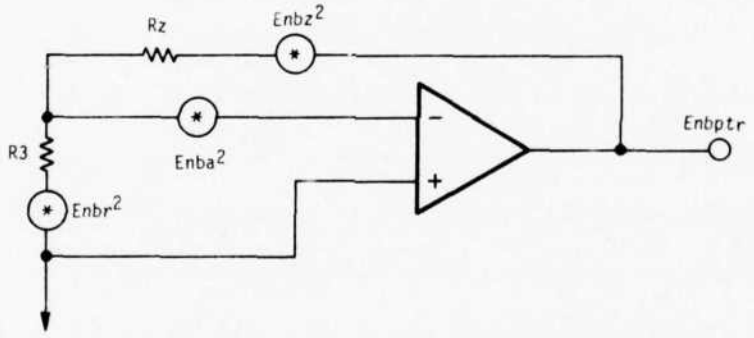


Figure B-6. +3.5 Vdc Regulator Noise Equivalent Circuit

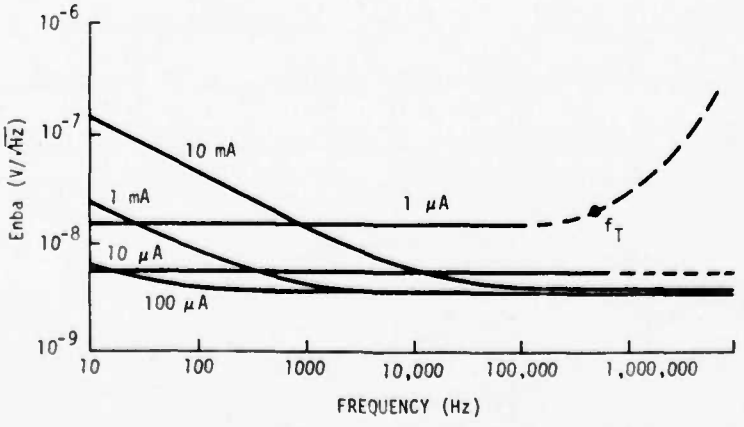


Figure B-7. Transistor 2N930 Noise Characteristics

The equations that relate the total output noise of the preamplifier regulator, Enbptr, are determined from Figure B-6 as follows:

$$Enbtpr = \left[\frac{Rz^2 \cdot Enbr^2}{R3^2} + \frac{(Rz + R3)^2}{R3^2} Enba^2 + Enbz^2 \right]^{1/2}$$

$R3 = 330 \qquad Rz \simeq 40$ ohms.

Therefore $Enbtpr = [7.8 \times 10^{-20} + 4526 \times 10^{-20} + 100 \times 10^{-20}]^{1/2}$

$$Enbtpr = 6.81 \text{ nV}/\sqrt{\text{Hz}}.$$

This value is the amount of noise that the preamplifier regulator places at the V_{CC} input of the preamplifier and is invariant with frequency.

If the narrowband noise is referenced to the input of the preamplifier, the noise will be attenuated greatly at dc (68 dB) and will be attenuated by only 8 dB in the range from 14 kHz to greater than f2, the system cutoff frequency. The total wideband noise, Ewbpr, at the output of the preamplifier regulator can be represented at the input to the preamplifier as shown in Figure B-8 and can be found by integrating the noise power density expression with the system frequency response as follows:

$$Ewbpr^2 = Enbpro^2 \left[\int_0^{f1} 10^{-6} \frac{f}{f1}\, df + \int_{f1}^{fA} 10^{-6}\, df + \int_{fA}^{fD} 10^{-6} \left(\frac{f}{fA}\right)^2 df + \int_{fD}^{f2} df + \int_{f2}^{\infty} \left(\frac{f2}{f}\right)^4 df \right]$$

where

f1 = 7 Hz = lower cutoff frequency (36 dB/octave)

f2 = 80 kHz = upper cutoff frequency (24 dB/octave)

fA = 20 Hz = (See Figures B-8 and B-5)

fD = 14 kHz = (See Figures B-8 and B-5)

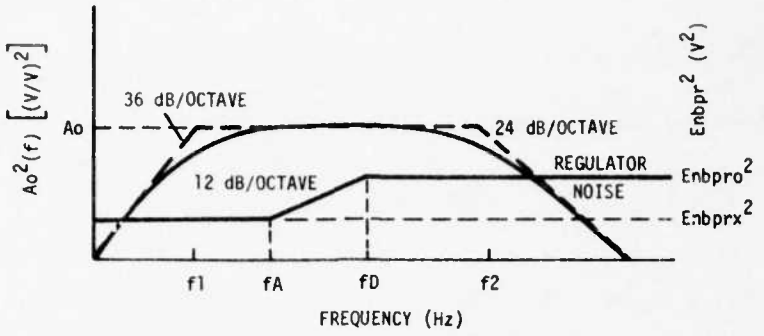


Figure B-8. Preamplifier Regulator Noise Equivalent and Video Electronics Response

$Enbpro^2 = (6.81\ nV/8\ dB)^2 = 7.36 \times 10^{-18}\ V^2/Hz$ (Preamplifier regulator maximum noise at minimum rejection)

$Enbrx^2 = Enbro^2 \times 10^{-6}\ V^2/Hz$ where Enbrx = low frequency regulator noise (Figure B-8)

$$Ewbpr^2 = Enbpro^2 \left[\frac{10^{-6} f^2}{7 f1} \Bigg|_{0\ Hz}^{7\ Hz} + 10^{-6} f \Bigg|_{7\ Hz}^{20\ Hz} + \frac{10^{-6} f^2}{2 fA} \Bigg|_{20\ Hz}^{14\ kHz} + f \Bigg|_{14\ kHz}^{80\ kHz} + \frac{f2^4 f^{-3}}{4} \Bigg|_{80\ kHz}^{\infty} \right]$$

$$Ewbpr^2 \simeq Enbpro^2 \left[\frac{10^{-6} (fD - fA)^2}{2fA} + (f2 - fD) + \frac{f2}{4} \right]$$

$$Ewbpr^2 \simeq Enbpro^2 [1.25\ f2 - fD] \simeq [1.25\ (80\ kHz) - 14\ kHz]\ Enbpro^2$$

$$Ewbpr^2 = 6.34 \times 10^{-13}\ V^2$$

$$Ewbpr = 0.796\ \mu V.$$

This is the noise present at the preamplifier output. When reflected to the input, the contribution is 0.011 μV and thus is negligible.

B.6 Preamplifier Ripple

The ripple appearing on the preamplifier module power leads, Er of Figure B-1, is attenuated by the preamplifier regulator and the preamplifier as shown by Curves A and B of Figure B-5, respectively. The composite rejection is

shown as Curve C and demonstrates a minimum of 90 dB of rejection around 30 kHz. If this minimum rejection is used to determine the allowable ripple at the preamplifier regulator input, the following is obtained:

$$Epr = \frac{Er}{90\ dB}$$

$$Epr = \frac{1\ mV}{90\ dB} = 3.1 \times 10^{-8}\ V$$

where 1 mV is the ripple of the +10 Vdc No. 1 (Figure 3.4-20) of the power supply determined by the bias regulator requirements of section B.8. Budgeting a tolerable level of 0.2 μV of ripple of the preamplifier input, the maximum ripple acceptable at the preamplifier regulator input is:

$$Epr\ (max) = 0.2\ \mu V \cdot 90\ dB = 6.3\ mV.$$

B.7 Detector Noise

The noise spectral density for the detector has been defined to be as shown in Figure B-4 with a 1/f noise rollup occurring at a 500 Hz break frequency. This 1/f contribution will be considered to be insignificant as described in section B.3, and only the white noise will be considered. The expression for determining the broadband noise of the detector is:

$$N_D = \frac{R(V/W)\ \sqrt{Ad(cm^2)}}{D^*(cm \cdot Hz^{1/2}/W)}\ .$$

Using specified nominal values as described in paragraph 3.1.2:

$$N_D = 2.9\ \frac{nV}{\sqrt{Hz}}\ .$$

Note: Although the geometry of the detector is classified, the area is not. The wideband noise contribution can be calculated using the noise bandwidth determined in section B.2 as follows:

$$Ewbd = N_D \sqrt{fn}$$

$$Ewbd = 0.84\ \mu V.$$

This is the value as presented in section 3.1.2 for the detector nominal noise level, N_D, based on minimum average specified responsivity and D*. Actual values may be significantly higher.

B.8 Detector Bias Regulator Noise

The detector bias regulator generates noise which is attenuated by the bias network of the detector by the ratio of $\frac{RD}{RB + RD}$ as shown in Figure B-1. This network also attenuates any ripple appearing at the input to the module as described in section B.9.

The equivalent circuit for determining the noise contribution of the bias regulator is shown in Figure B-9, and the noise sources are identified as:

$Enbo21^2$ - noise contribution of R21

$Enbo18^2$ - noise contribution of R18

$Enbo23^2$ - noise contribution of R23'

$Enboz^2$ - noise contribution of CR7 (I = 2 mA)

$EnboQ8^2$ - noise contribution of Q8 (I = 1 mA)

$EnboQ9^2$ - noise contribution of Q9 (I = 1 mA)

The narrowband noise term contribution at the output due to each source is as follows:

$$Enbz^2 = 2q(Idc)\ Rz^2 \left[\frac{(R21)\ (R18 + R23')}{R23'\ R21 - Rz\ R18}\right]^2$$

$$Enb18^2 = 4KT(R18) \left[\frac{R23'\ (R21 + Rz)}{R23'\ R21 - Rz\ R18}\right]^2$$

$$Enb21^2 = 4KT(R21) \left[\frac{Rz\ (R18 + R23')}{R23'\ R21 - Rz\ R18}\right]^2$$

$$Enb23^2 = 4KT(R23') \left[\frac{R18\ (Rz + R21}{R23'\ R21 - Rz\ R18}\right]^2$$

$$EnbQ8^2 = enboQ8^2 \left[\frac{(R18 + R23')\ (R21 + Rz)}{R23'\ R21 - Rz\ R18}\right]^2$$

$$EnbQ9^2 = enboQ9^2 \left[\frac{(R18 + R23')\ (R21 + Rz)}{R23'\ R21 - Rz\ R18}\right]^2.$$

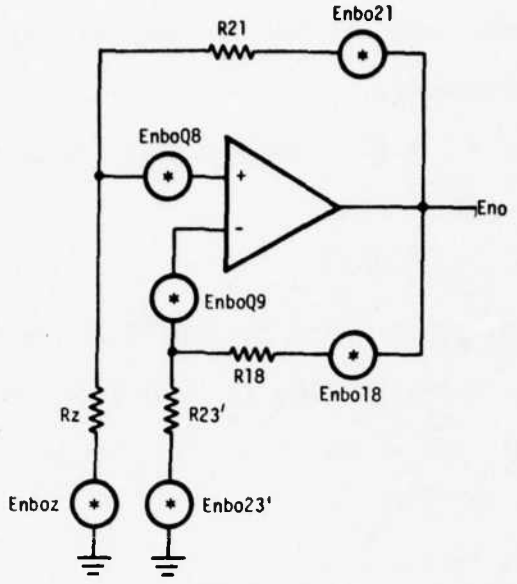


Figure B-9. Bias Regulator Equivalent Noise Circuit

These equations can be solved using the following values for the components:

Rz = 40 ohms

R18 = 649 ohms

R21 = 1000 ohms

R23' = 400 ohms (R23 in parallel with R24)

EnbQ8 = EnbQ9 = 307 x 10^{-18} V^2/Hz (taken from the curves of Figure B-7 for the 2N930 transistor).

Solving:

$Enbz^2$ = 8.6 x 10^{-18} V^2/Hz

$Enb18^2$ = 12.93 x 10^{-18} V^2/Hz

$Enb21^2$ = 8.10 x 10^{-20} V^2/Hz

$Enb23^2$ = 2.10 x 10^{-17} V^2/Hz

$EnbQ8^2$ = 307 x 10^{-18} V^2/Hz

$EnbQ9^2$ = 307 x 10^{-18} V^2/Hz.

The total output noise of the bias regulator is the root-sum-square sum of the six contributors.

$$Enbbr^2 = Enbz^2 + Enb21^2 + Enb18^2 + Enb23^2 + EnbQ8^2 + EnbQ9^2$$

$$Enbbr^2 = 657 \times 10^{-18}\ V^2/Hz$$

$$Enbbr = 25.6 \times 10^{-9}\ V/\sqrt{Hz}.$$

The total noise appearing at the output of the bias regulator over the complete range of interest, Ewbbr, is found by multiplying the narrowband noise by the square root of the noise bandwidth to obtain:

$$Ewbbr = Enbbr \sqrt{81.2\ kHz}$$

$$Ewbbr = 7.29 \times 10^{-6}\ V.$$

This appears as a noise source at the input to the preamplifier and can be determined by the following expression:

$$Ewbb^2 = Ewbbr^2 \left(\frac{RD}{RD + RB}\right)^2$$

$$Ewbb = 0.178\ \mu V.$$

B.9 Detector Bias Regulator Ripple

As was assumed for the preamplifier, the allowable noise contribution of the detector biasing circuitry and ripple will be estimated to be 0.2 μV as viewed at the input to the preamplifier. Because any noise or ripple at the input to the detector module is attenuated by RD/(RD + RB) as shown in Figure B-1, the allowable ripple and noise out of the bias regulator can be calculated to be:

$$Ewbtbr = \frac{RD + RB}{RB}\ (0.2\ \mu V)$$

$$Ewbtbr = \frac{(50 + 2k)}{50}\ 0.2\ \mu V = 8.2\ \mu V.$$

Because the bias regulator contributes 7.29 μV of noise, the amount that can be allocated to the ripple output from the bias regulator, Ewbrb, is:

$$Ewbrb = [Ewbtbr^2 - Ewbbr^2]^{1/2}$$

$$Ewbrb = [8.2^2 - 7.29^2]^{1/2}\ \mu V$$

$$Ewbrb = 3.75\ \mu V.$$

This is referenced to the input of the preamplifier as follows:

$$Ewbr^2 = Ewbrb^2 \left(\frac{RD}{RD + RB}\right)^2 = 8.37 \times 10^{-15}$$

$$Ewbr = 0.09 \times 10^{-6}.$$

This can be related to the input of the bias regulator by the power supply rejection of the bias regulator which was determined by analysis and is as shown in Figure B-10. Assuming a conservative minimum rejection of 54 dB, the allowable ripple at the input to the bias regulator is:

$$Er = Ewbrb \times 54\ dB$$

$$Er = (3.75\ \mu V)\ (500) = 1.875\ mV.$$

This level of ripple establishes the requirement of 1 mV used in the design of the power supply of paragraph 3.4.3.

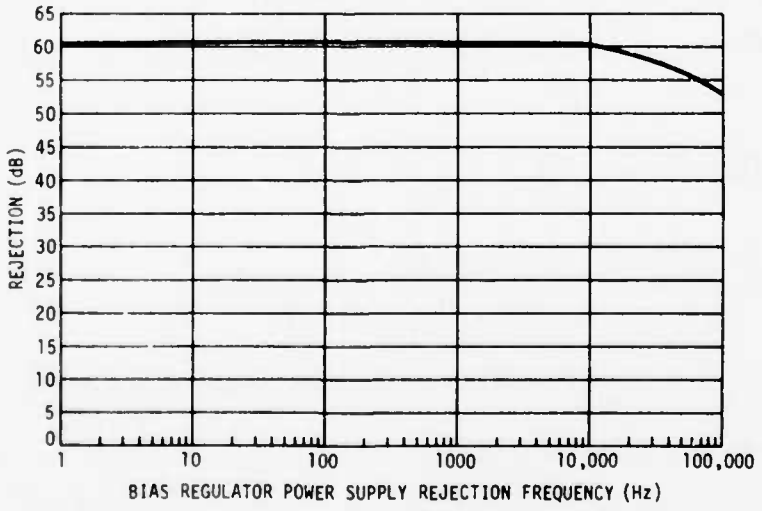


Figure B-10. Bias Regulator Power Supply Rejection

B.10 Postamplifier Noise

In a multistage amplifier system as shown in Figure B-1, the noise of the input stage is the prime contributor because the second stage contribution is divided by the gain of the first stage when referred to the first stage input. Because the gain of the first stage is not relatively high, a cursory analysis should be provided to ensure that the second stage is not a prime contributor.

Three potential sources of amplifier noise contribute to equivalent input noise. These are: 1) the first stage postamplifier, 2) the second stage postamplifier, and 3) the LED driver. To achieve the required dynamic range, it is necessary for each postamplifier gain-controlled stage to have maximum to minimum gain control. The worst-case noise occurs at minimum gain. However, since minimum gain of each postamplifier stage is 8, and the preamplifier gain is 70, the LED driver noise is reduced by a gain of 4480 and thus is negligible.

The equivalent input noise of each postamplifier is 25 nV/Hz at the IC input. Reflecting each noise to the preamplifier input yields the following noise contributions for the first and second postamplifier stages:

First stage noise = E_{WBA1}

$$E_{WBA1} = \frac{25 \text{ nV/ Hz} \times 1.57 f_{H1}}{70} = 0.148\mu V$$

f_{H1} = postamplifier high frequency response = 110 kHz

Second stage noise = E_{WBA2}

$$E_{WBA2} = \frac{25 \text{ nV/ Hz} \times 1.57 \text{ fHz}}{70 \times 8} = 0.066 \ \mu V$$

fHz = second stage high frequency response = 1.4 MHz.

The only contribution of the second stage that is considered is the ripple, which is a function of the regulator for the postamplifier located within the auxiliary control module. The noise generated by the auxiliary control regulators will be considered insignificant in view of the results of the preamplifier regulator and bias regulator noise levels which were less than 10 μV over the frequency range of interest. If the auxiliary control (+) and (-) regulators were 10 μV and the postamplifier power supply rejection were 0 dB (a conservative estimate), its contribution at the preamplifier input would be 10 μV/70 = 0.14 μV, which is negligible.

The ripple rejection offered by the (+) and (-) supplies are considered to be identical for this analysis due to the similarity in the two regulator designs. The ripple rejection of the auxiliary control was determined by computer analysis to be as shown by Curve A in Figures B-11 and B-12 for the (+) and (-) auxiliary control regulators. Curve B of Figure B-11 is the ripple rejection of the V_{CC} input. Curve C of the same figure is the composite of Curves A and B and is a minimum of 91 dB at 100 kHz. At a typical converter operating frequency of 20 kHz, the typical ripple rejection is 96 dB as viewed at the input to the postamplifier.

Similarly, the curves of Figure B-12 were generated for the V_{EE} input to the preamplifier and exhibit a rejection of 93 dB at 20 kHz. If 0.2 μV was the noise budgeted at the input to the preamplifier, this reflects as (0.2 μV) 0.70 = 14 μV at the input to the postamplifier. This demonstrates a tolerable ripple level, Erx or Ery as shown in Figure B-1, of:

Erx = 14 μV · 96 dB = 883 mV

Ery = 14 μV · 93 dB = 625 mV.

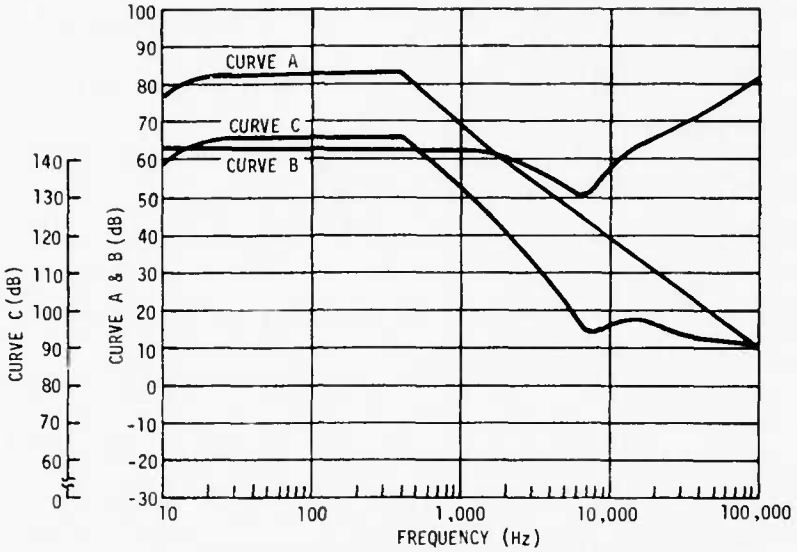


Figure B-11. Postamplifier/(+) Auxiliary Regulator Ripple Rejection Characteristics

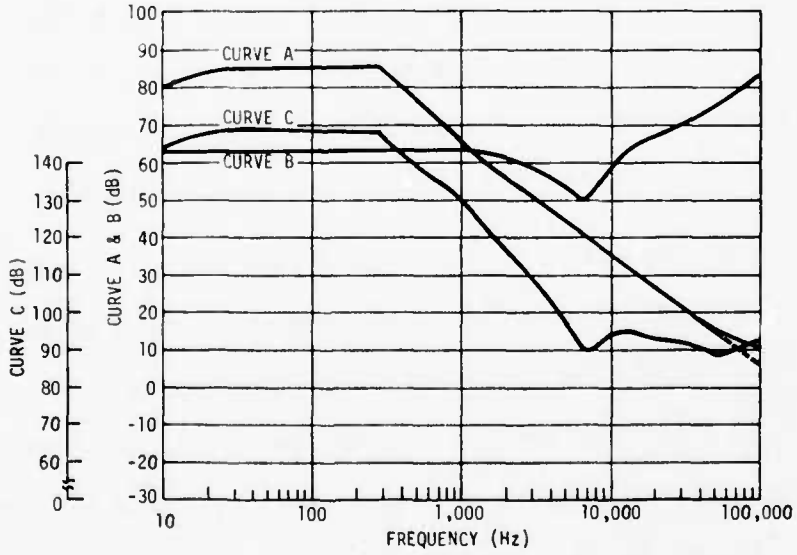


Figure B-12. Postamplifier/(-) Auxiliary Regulator Ripple Rejection Characteristics

This demonstrates that the ripple input to the auxiliary control regulator is not a critical requirement with respect to its contributions to the total noise of the system.

B.11 Noise Analysis Summary

As can be determined from the analyses of this appendix, the total noise for a particular system is uniquely defined by that system, and the analysis procedures developed must be adapted to meet these requirements.

The noise bandwidth analysis of section B.2 demonstrated that two noise bandwidths were to be considered when the bandwidth was electronics-limited and depended on the source of noise. The analysis was complicated by the fact that one noise bandwidth (fn) had an 18 dB/octave slope while the other noise bandwidth (fna) had a 12 dB/octave slope. In a system that does not use the full bandwidth determined by the electronics, it may be possible to represent all noise sources with the same noise bandwidth with relatively small error.

In section B.3, it was proven that when the full electronics bandwidth was used, the 1/f noise could be neglected. When the system bandwidth is reduced, the error becomes more prominant, and the 1/f may be a significant contributor. At a system bandwidth of 25 kHz, the 1/f source (f_B = 1 kHz) introduced an error of approximately 1.7 percent.

The preamplifier ripple analysis demonstrated that the preamplifier regulator and preamplifier ripple rejections were more than adequate, and the ripple at a typical converter frequency of 20 kHz was not significant.

The detector bias regulator noise was shown to provide less than 0.2 μV noise for noise bandwidths up to 81.2 kHz, while the ripple requirement for the input power was determined to be in the range of 1 mV. If lesser

bandwidths are used for a particular system, the allowable ripple of the bias regulator can be increased.

The ripple rejection of the second stage of amplification was examined and a minimal noise contribution from this source was demonstrated.

For the analyses of sections B.2 through B.10, the total noise (Ent) for the full electronics bandwidth can be determined to be:

$$Ent = \left[Ewbp^2 + Epr^2 + Ewbd^2 + Ewbb^2 + Ewbr^2 + Ewba^2 + Ewba_2 + Ewbar^2 \right]^{\frac{1}{2}}$$

$$Ent = \left[(0.469)^2 + (0.031)^2 + (0.840)^2 + (0.178)^2 \ (0.09)^2 + (0.148)^2 + + (0.066)^2 + (0.140)^2 \right]^{\frac{1}{2}}$$

$$Ent = 1.01 \ \mu v.$$

APPENDIX C

COMMON MODULE VIBRATION TESTING

C.1 General

Vibration tests were conducted on each of the common modules listed below as part of the Engineering Design Test Program under Contract DAAG53-75-C-0179. Testing was performed using the environmental test facilities at the Orlando, Florida, Division of the Martin Marietta Corporation:

1 Preamplifier (SM-D-773663)

2 Postamplifier (SM-D-773900)

3 Bias regulator (SM-D-773914)

4 Auxiliary control module (SM-D-773896)

5 IR imager (SM-D-804143)

6 Visual collimator (SM-D-773397)

7 Mechanical scanner (SM-D-773885)

8 Scan and interlace module (SM-D-773894), now obsolete configuration

9 Cooler (SM-D-773683)

10 Inverter (SM-D-773433).

The preamplifier, postamplifier, auxiliary control, and bias regulator modules were installed in a simulated system housing P/N 68400375 and exposed to the vibration environment as a video electronics group. The remaining modules were grouped for testing as follows:

1 Mechanical scanner and scan and interlace modules

2 IR imager and visual collimator

3 Cooler and inverter.

C.2 Vibration Test Levels

Vibration testing involved exposing the common modules to 3 hours of vibration in each axis. This exposure consisted of a 15-minute resonance search from 5 to 500 to 5 Hz, 30 minutes of resonance dwell at each of the resonances found (up to four), and a sine cycle test for the remainder of the 3 hour per axis requirement using the test levels shown in Figure C-1.

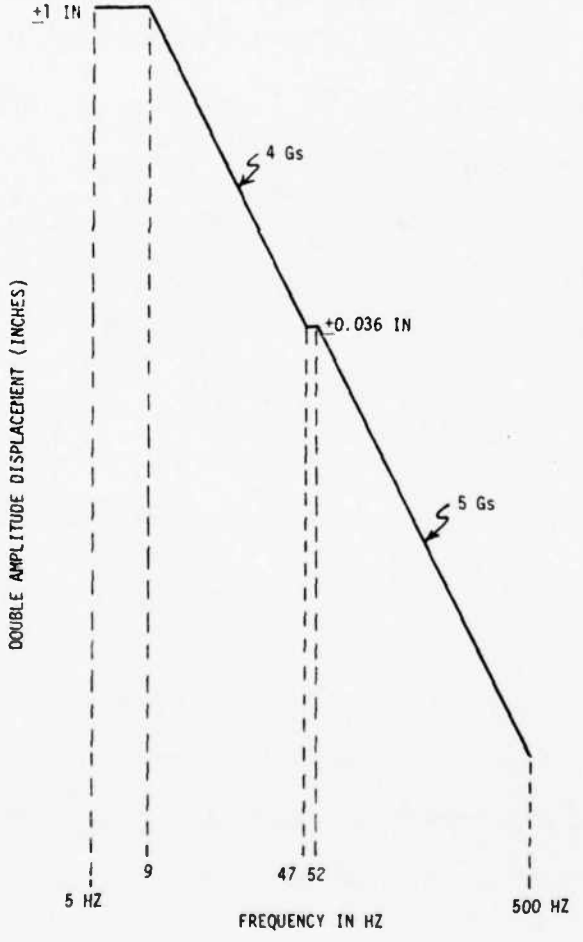


Figure C-1. Common Module Vibration Test Curve

C.3 Vibration Test Data

Common module response to the vibration environment was also recorded using the accelerometers shown in Table C-I and Figures C-2 through C-7. The accelerometer outputs were displayed on a Honeywell Model 1912 oscillograph recorder and stored on magnetic tape. The magnetic tape data from the resonance searches in each axis were fed into an SD 1002D-16B spectrum analyzer to assist in determining system resonances. Photographs defining the longitudinal, lateral I, and lateral II axis test orientations are documented in Figures C-8 through C-20, while the plots produced using the spectrum analyzer are shown in Figures C-21 through C-32. Resonance conditions determined using these plots are recorded in Table C-II.

TABLE C-I

Accelerometer Locations for Common Module Vibration Testing

Test Item	Accelerometer Type	Accelerometer Location	Remarks
Video Electronic Housing	Endevco 2228	Case exterior, side, long axis	Fig. C-2
Video Electronic Housing	Endevco 2228	Case exterior, side, lat I axis	
Video Electronic Housing	Endevco 2228	Case exterior, side, lat II axis	
Preamplifier	Endevco 22	Back near connector, long axis	
Preamplifier		Back near connector, lat I axis	
Preamplifier		Back near connector, lat II axis	
Postamplifier	Back near	Back near connector, long axis	
Postamplifier		Back near connector, lat I axis	
Postamplifier		Back near connector, lat II axis	
Mechanical Scanner		Top frame near corner, long axis	Fig. C-3
Mechanical Scanner		Top frame near corner, lat I axis	Fig. C-3
Mechanical Scanner		Top frame near corner, lat II axis	Fig. C-3
Scan/Interlace Assembly		Board connector, long axis	Fig. C-4
Scan/Interlace Assembly		Board connector, lat I axis	Fig. C-4
Scan/Interlace Assembly		Board connector, lat II axis	Fig. C-4
Cooler		Side of cooler casting, long axis	Fig. C-5
Cooler		Side of cooler casting, lat I axis	Fig. C-5
Cooler		Side of cooler casting, lat II axis	Fig. C-5
Inverter		Inside near top corner, long axis	Fig. C-6
Inverter		Inside near top, lat I axis	Fig. C-6
Inverter		Inside near top, lat II axis	Fig. C-6
IR Imager		Housing, near end opposite flange, long axis	Fig. C-7
IR Imager		Housing, near end opposite flange, lat I axis	
IR Imager		Housing, near end opposite flange, lat II axis	
Visual Collimator		Housing, near end opposite flange, long axis	
Visual Collimator		Housing, near end opposite flange, lat I axis	
Visual Collimator	Endevco 22	Housing, near end opposite flange, lat II axis	Fig. C-7

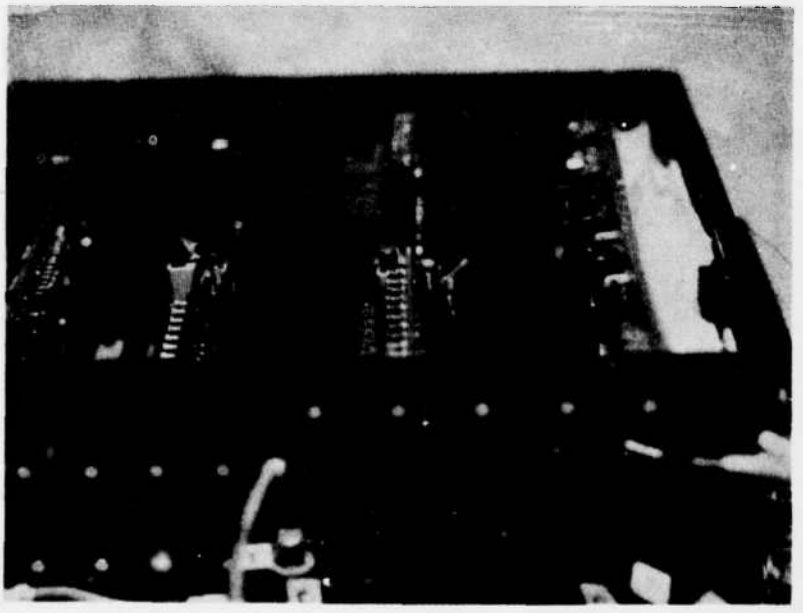


Figure C-2. Location of Accelerometers for Video Electronics Vibration and Shock Tests

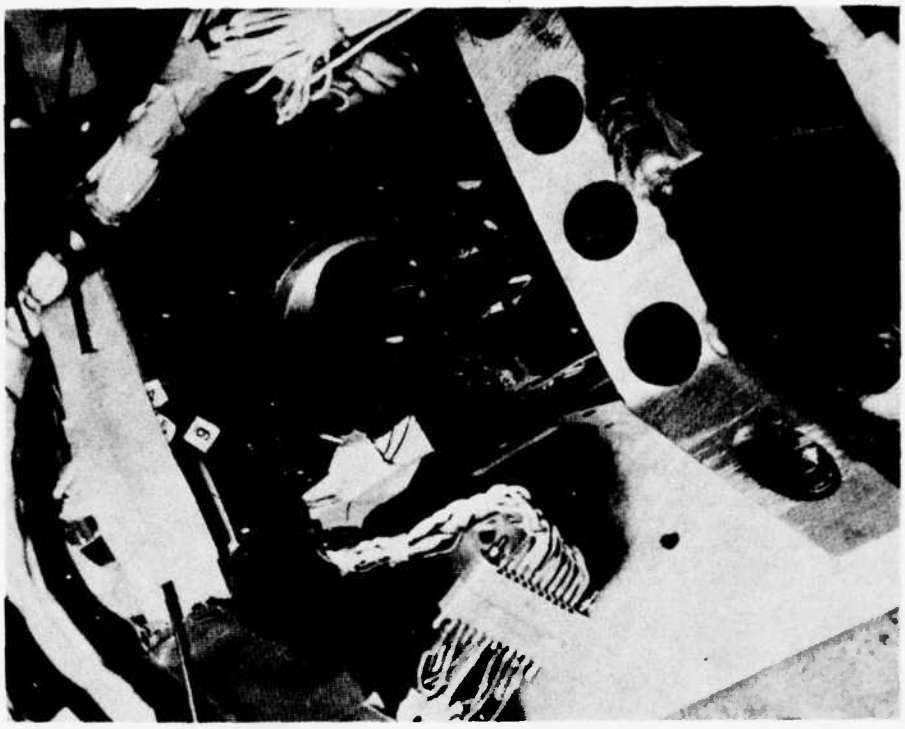


Figure C-3. Location of Accelerometers
for Mechanical Scanner Vibration
and Shock Tests

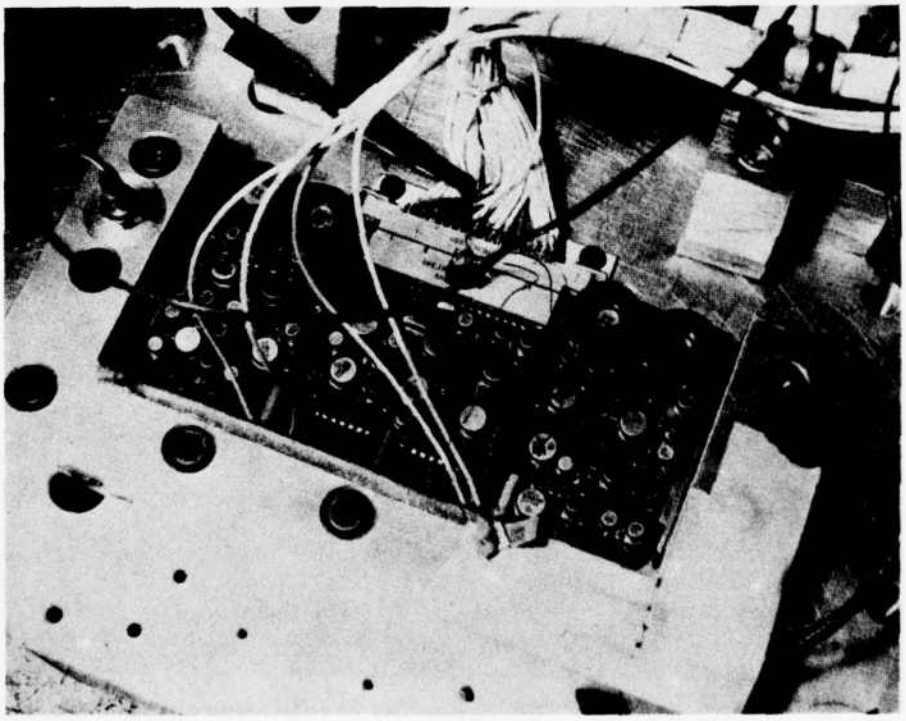


Figure C-4. Location of Accelerometers
for Scan Interlace Card Vibration
and Shock Tests

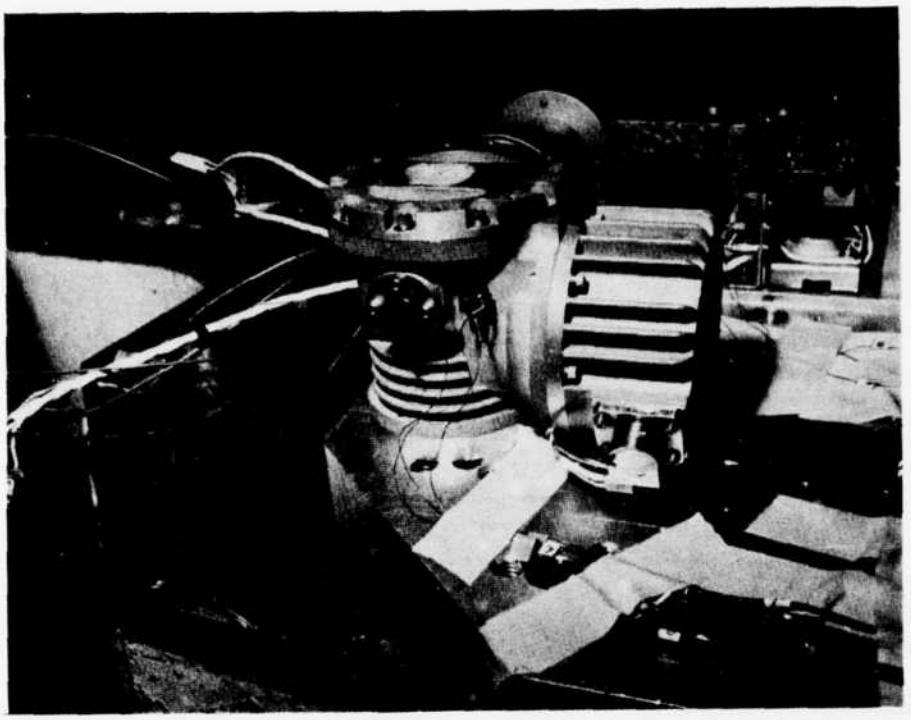


Figure C-5. Location of Accelerometers
for Cooler Vibration
and Shock Tests

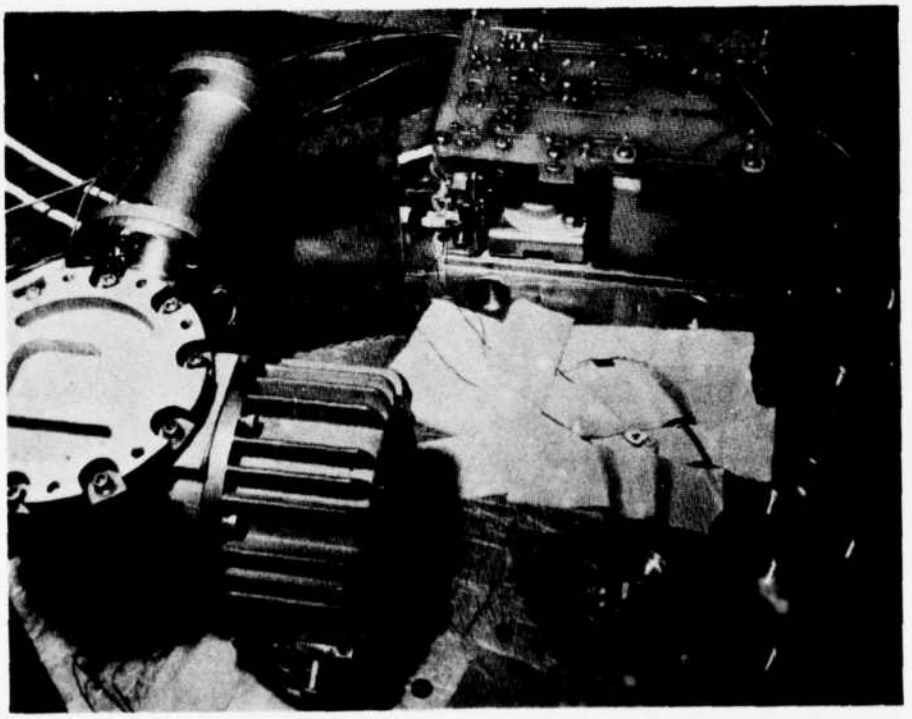


Figure C-6. Location of Accelerometers
for Inverter Vibration
and Shock Tests

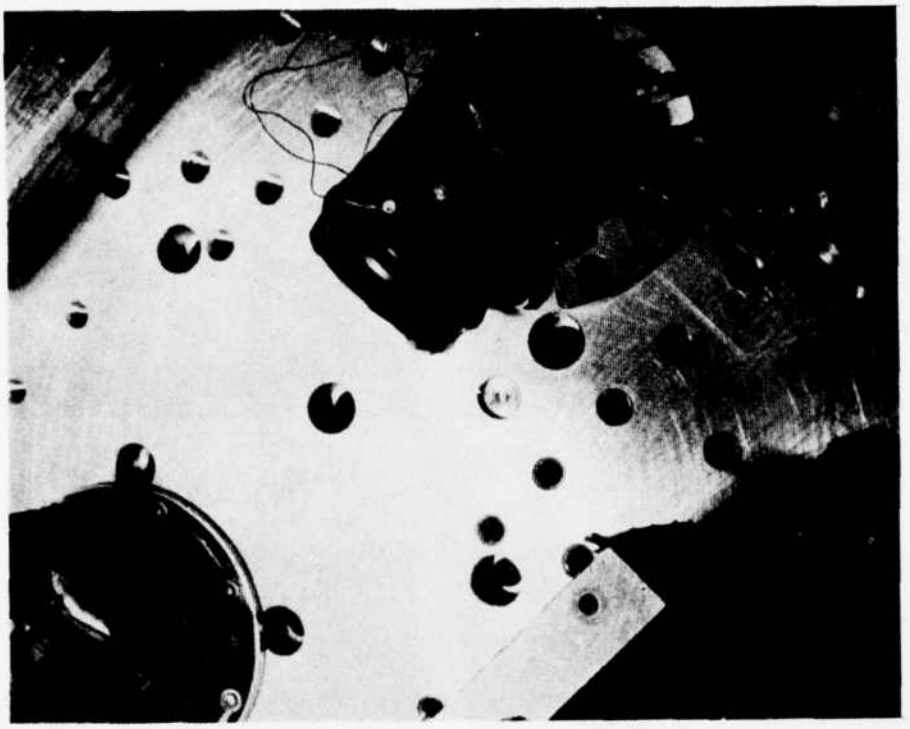


Figure C-7. Location of Accelerometers for Imager and Collimator Vibration and Shock Tests

Figure C-8. Video Electronics Longitudinal Axis Installation, 10 August 1976

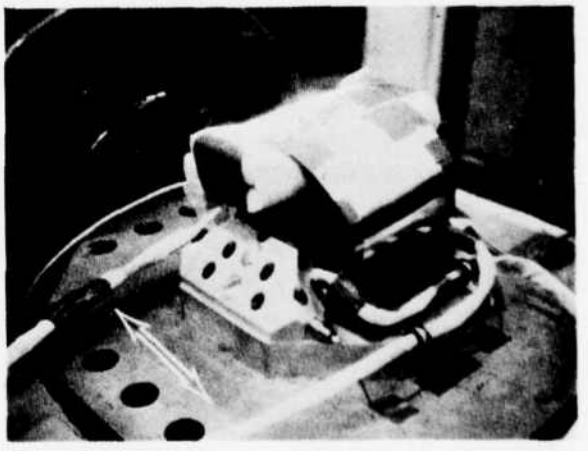


Figure C-9. Video Electronics Installation, Lateral II Axis with Conetic Shield, 12 August 1976

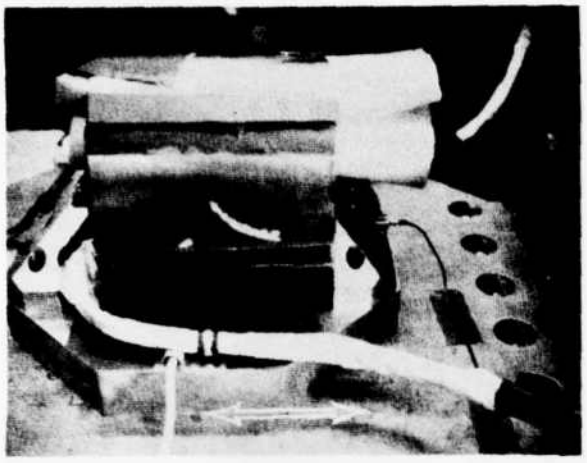


Figure C-10. Video Electronics Installation, Lateral I Axis with Conetic Shield, 13 August 1976

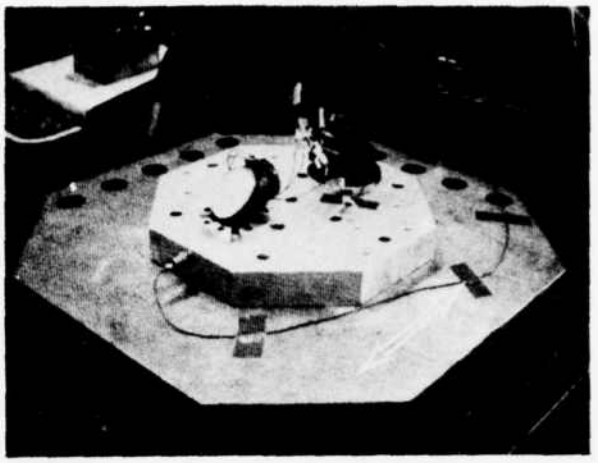


Figure C-11. Vibration of Optical Modules, Lateral I Axis, 27 August 1976

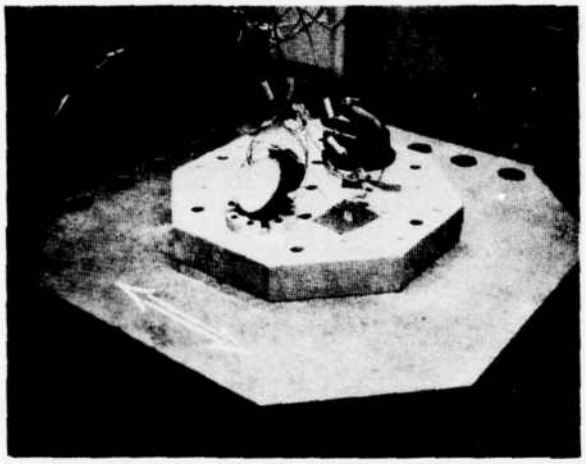


Figure C-12. Vibration of Optical Modules, Lateral II Axis, 30 August 1976

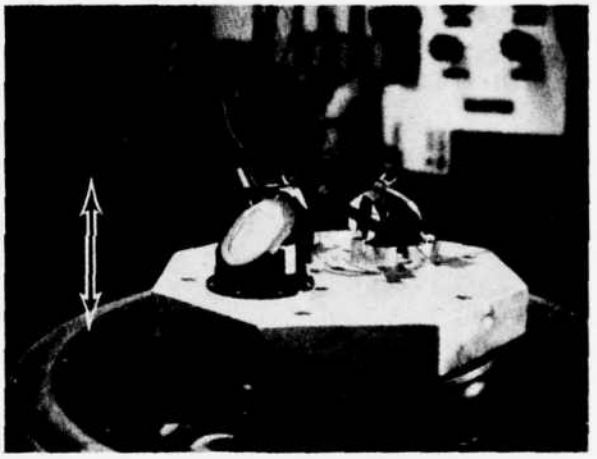


Figure C-13. Vibration of Optical Modules, Longitudinal Axis, 30 August 1976

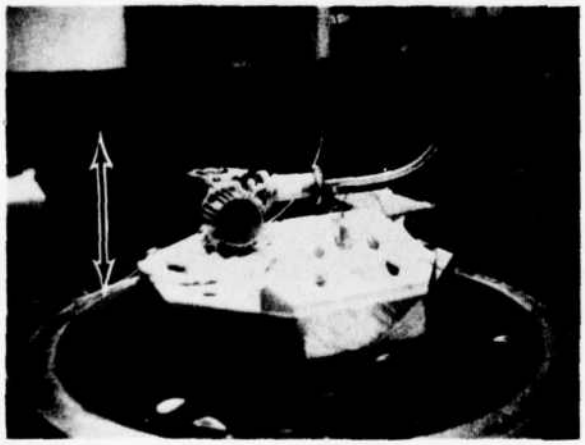


Figure C-14. Cooler/Inverter Vibration, Longitudinal Axis, 13 September 1976

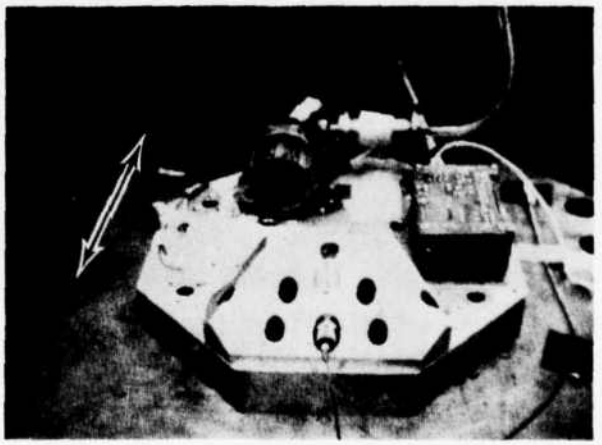


Figure C-15. Cooler/Inverter Vibration, Lateral I Axis, 14 September 1976

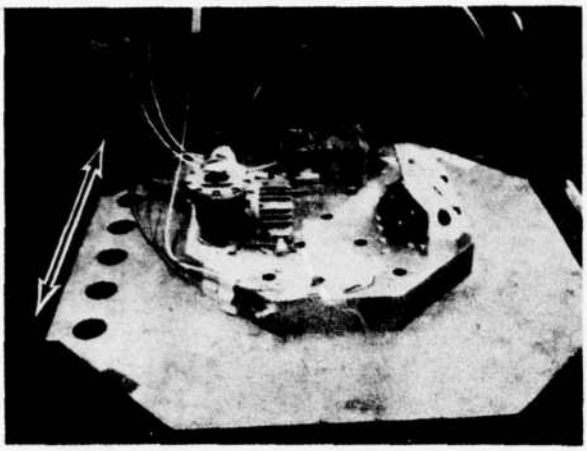


Figure C-16. Cooler/Inverter Vibration, Lateral II Axis, 14 September 1976

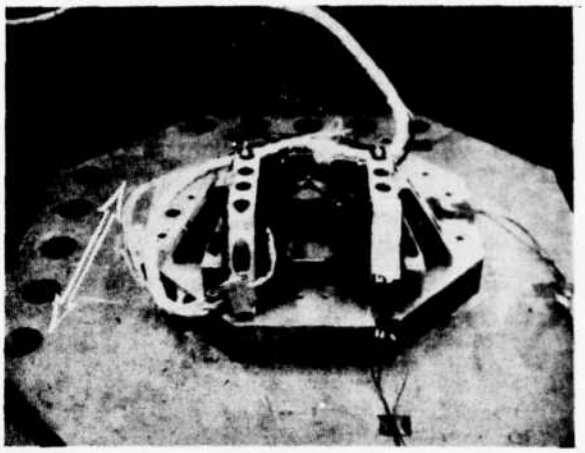


Figure C-17. Scan Mechanism Vibration, Lateral II Axis, 18 September 1976

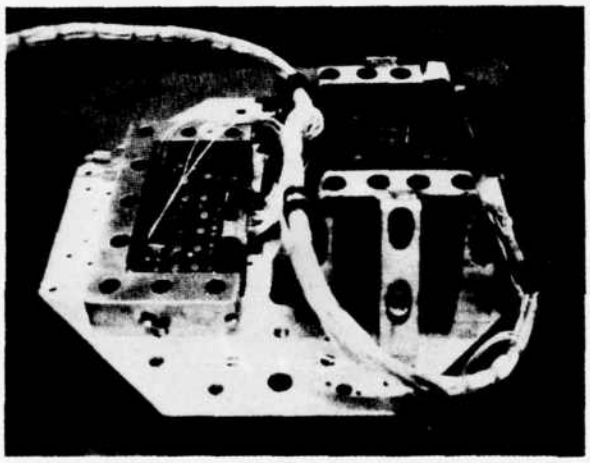


Figure C-18. Scan Mechanism Vibration, Lateral II Axis, 18 September 1976

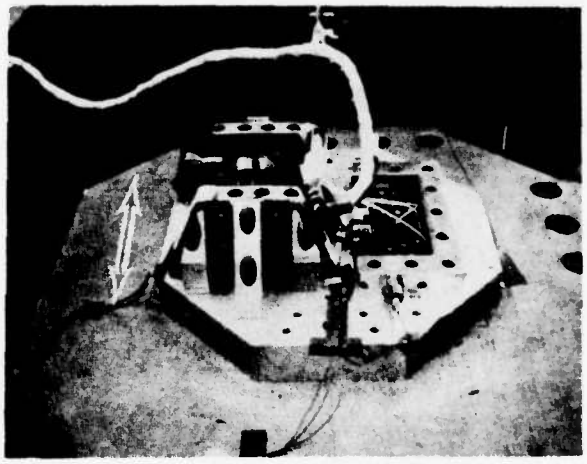


Figure C-19. Scan Mechanism Vibration, Lateral I Axis, 19 September 1976

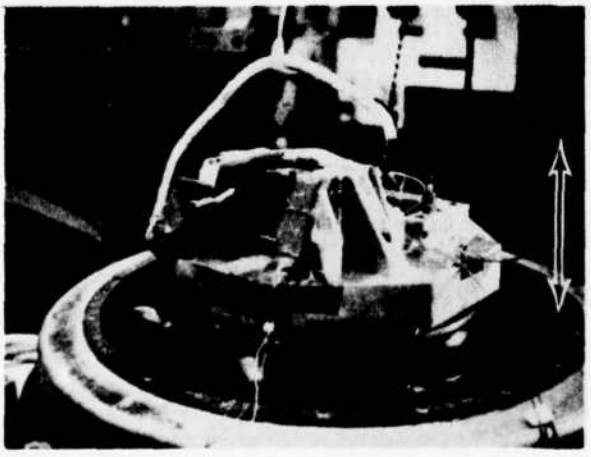


Figure C-20. Scan Mechanism Vibration, Longitudinal Axis, 19 September 1976

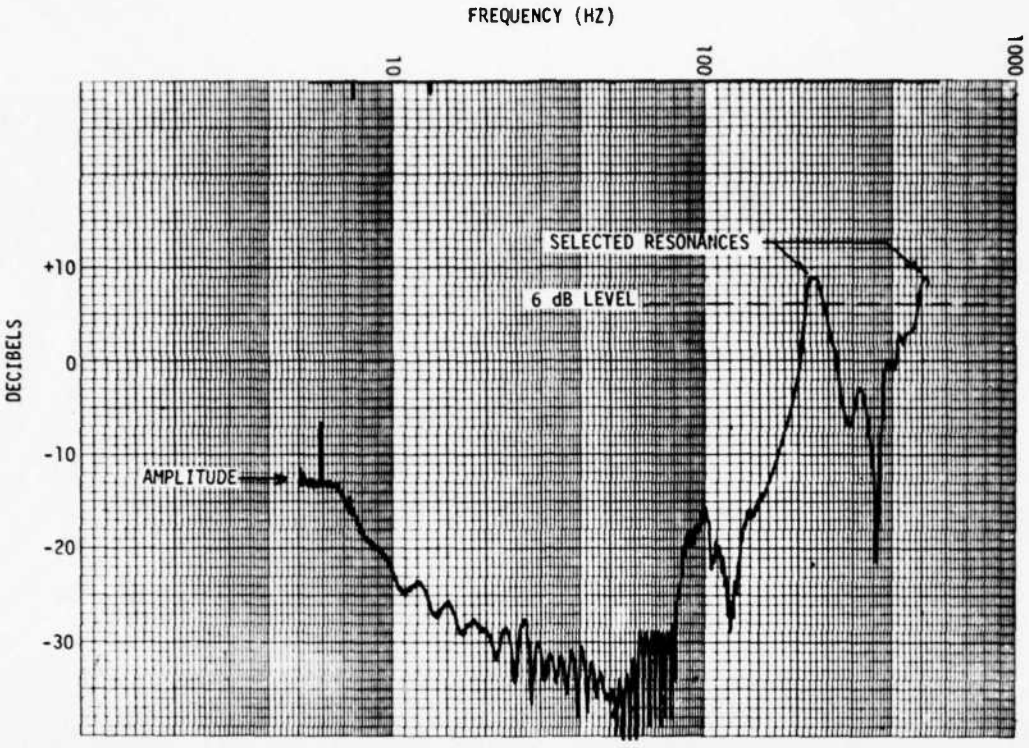


Figure C-21. Spectum Analysis Plot, Preamplifier Lateral I Response/ Control, Longitudinal Axis Vibration, Full-Level Run, 11 August 1976

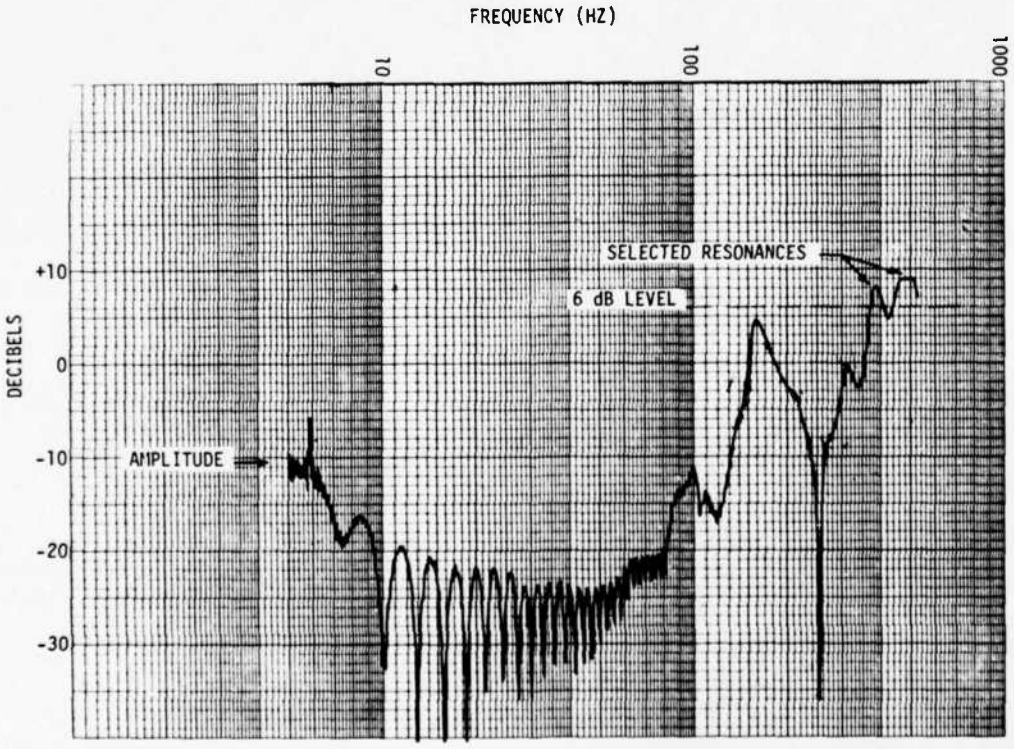


Figure C-22. Spectrum Analysis Plot, Postamplifier Lateral I Response/ Control, Longitudinal Axis Vibration, Full-Level Run, 11 August 1976

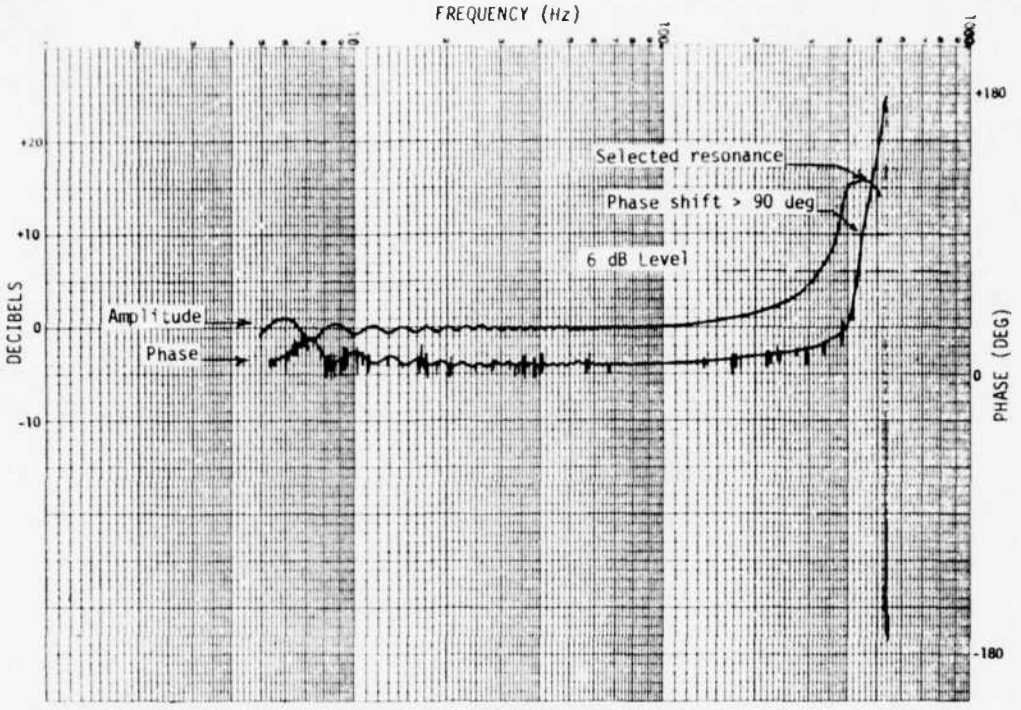


Figure C-23. Spectrum Analysis Plot, Postamplifier Lateral II Response/ Control, Lateral II Axis Vibration, Full-Level Run, 12 August 1976

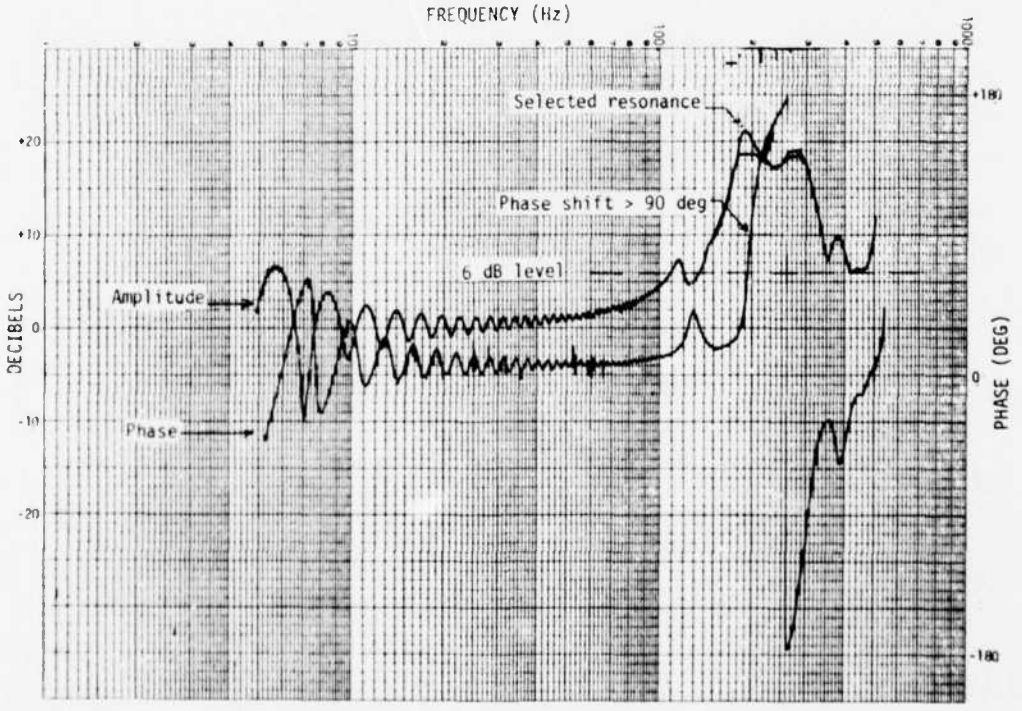


Figure C-24. Spectrum Analysis Plot, Preamplifier Lateral I Response/ Control, Lateral I Axis Vibration, Full-Level Run, 13 August 1976

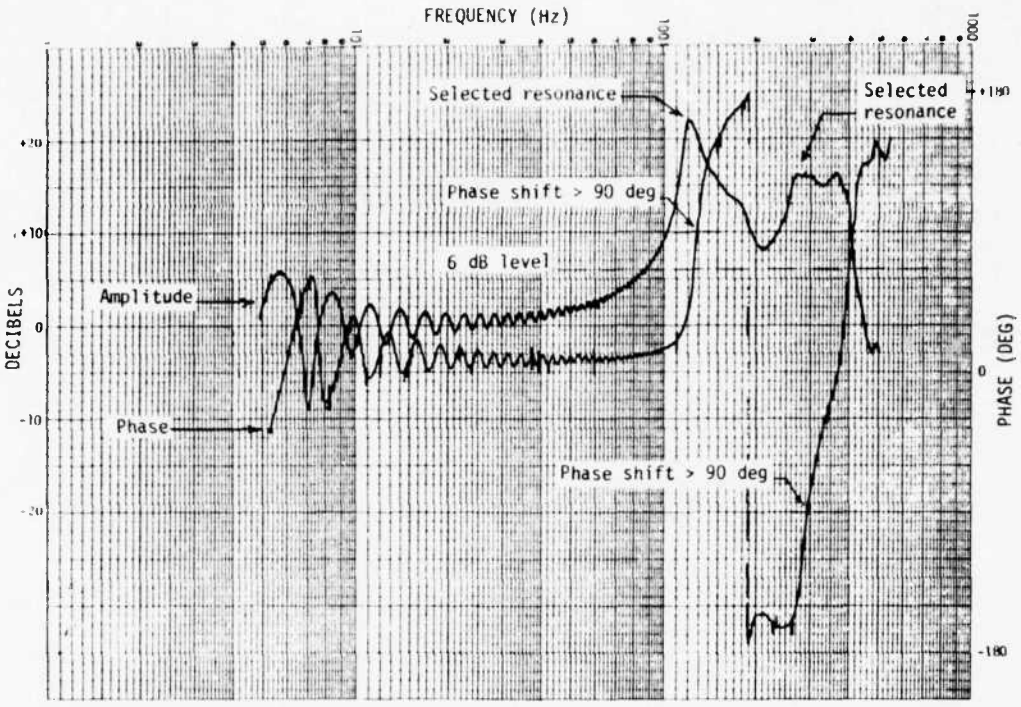


Figure C-25. Spectrum Analysis Plot, Postamplifier Lateral I Response/ Control, Lateral I Axis Vibration, Full-Level Run, 13 August 1976

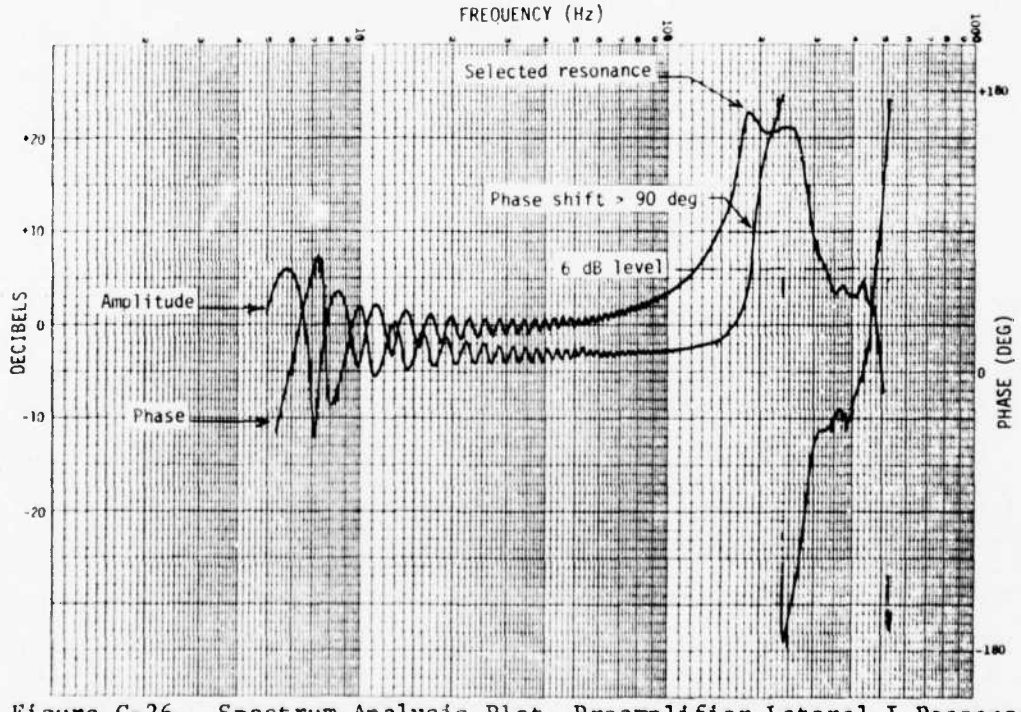


Figure C-26. Spectrum Analysis Plot, Preamplifier Lateral I Response/ Control, Lateral I Axis Vibration, Run No. 3 at Full Level, 18 August 1976

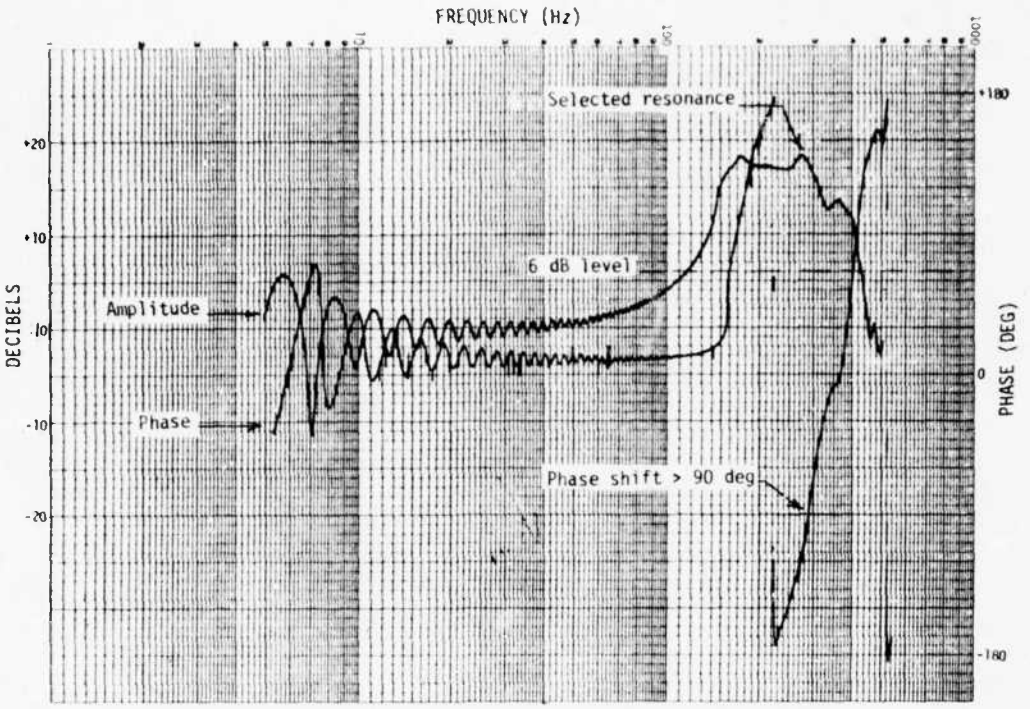


Figure C-27. Spectrum Analysis Plot, Postamplifier Lateral I Response/ Control, Lateral I Axis Vibration, Run No. 3 at Full Level, 18 August 1976

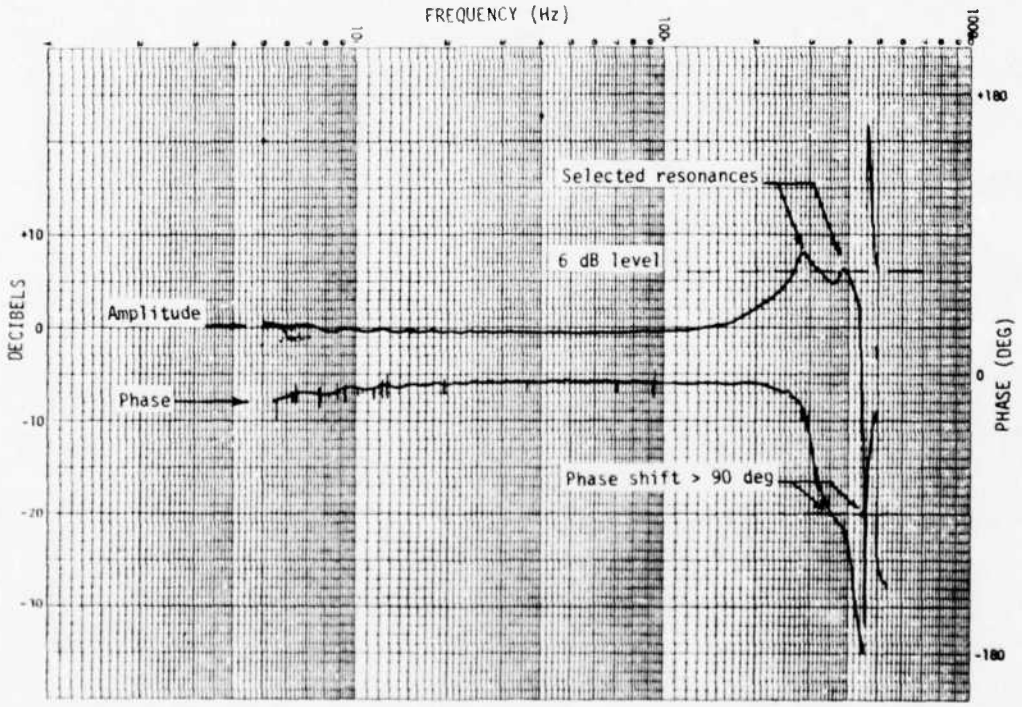


Figure C-28. Spectrum Analysis Plot, Scan and Interlace Assembly Longitudinal Response/Control, Longitudinal Axis Vibration, Full-Level Run, 19 September 1976

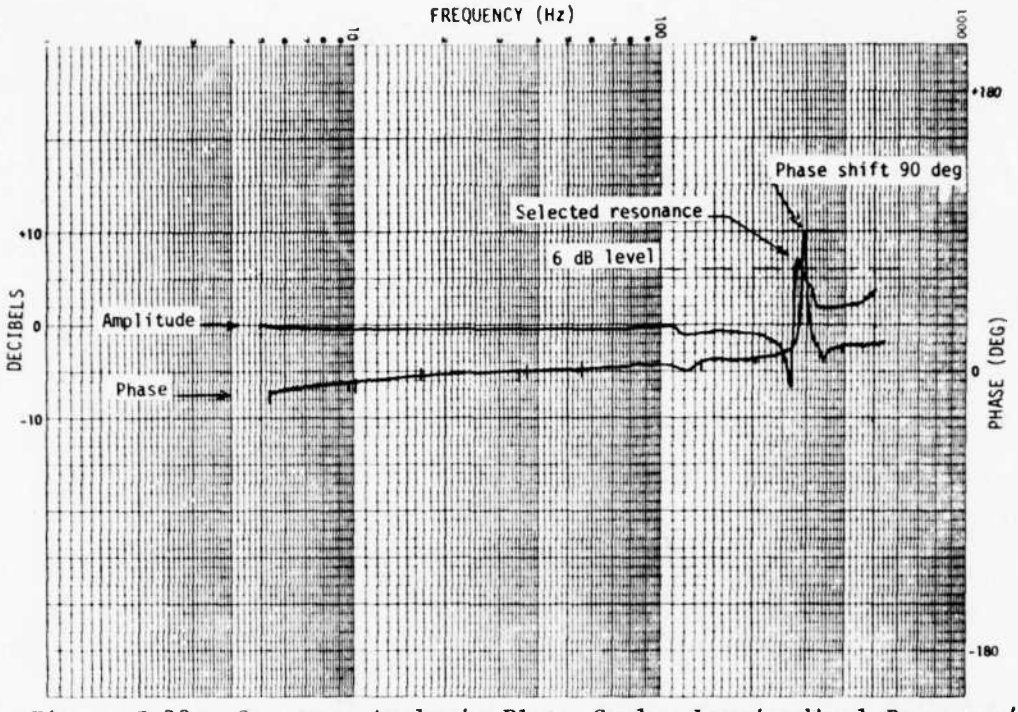


Figure C-29. Spectrum Analysis Plot, Cooler Longitudinal Response/ Control, Longitudinal Axis Vibration, Full-Level Run, 13 September 1976

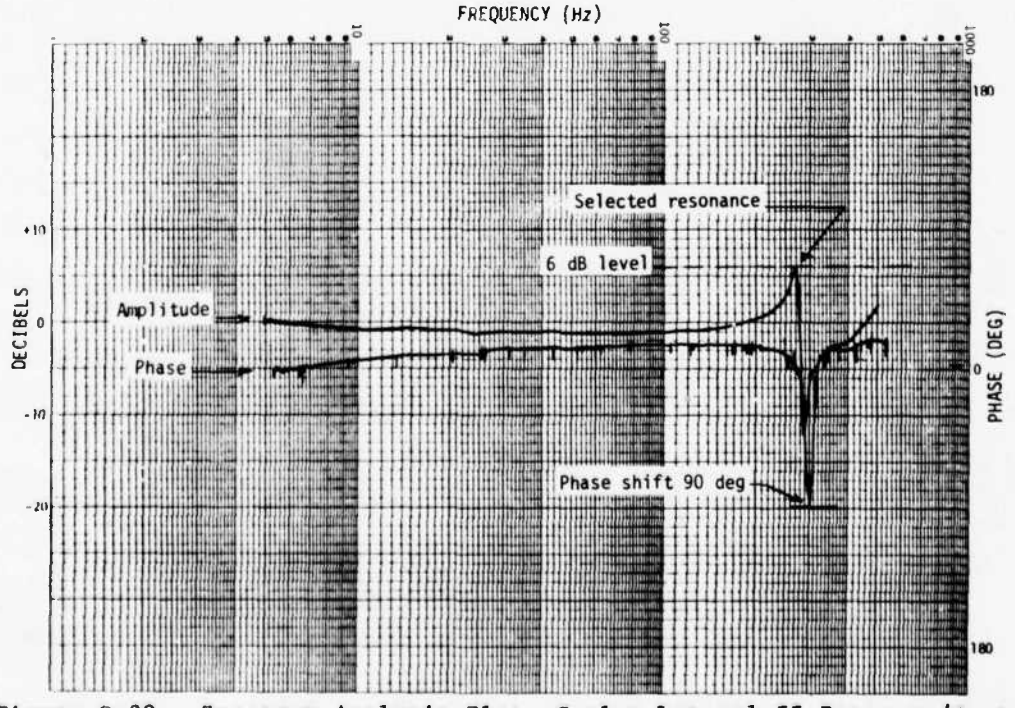


Figure C-30. Spectrum Analysis Plot, Cooler Lateral II Response/Control, Lateral II Axis Vibration, Full-Level Run, 14 September 1976

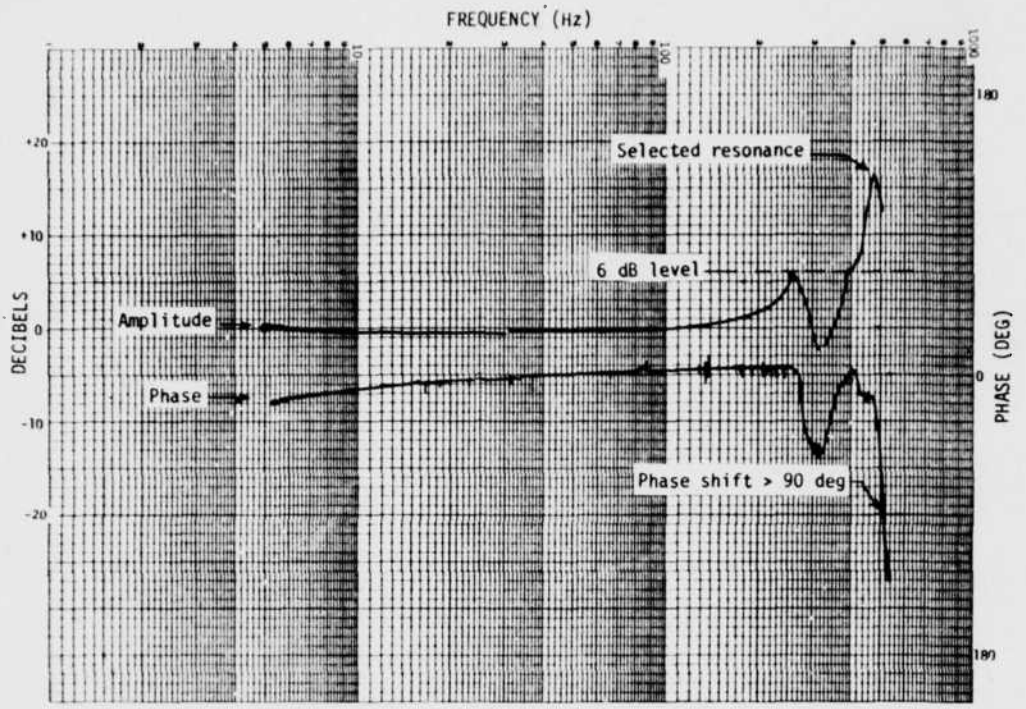


Figure C-31. Spectrum Analysis Plot, Inverter Lateral I Response/Control, Lateral I Axis Vibration, Full-Level Run, 14 September 1976

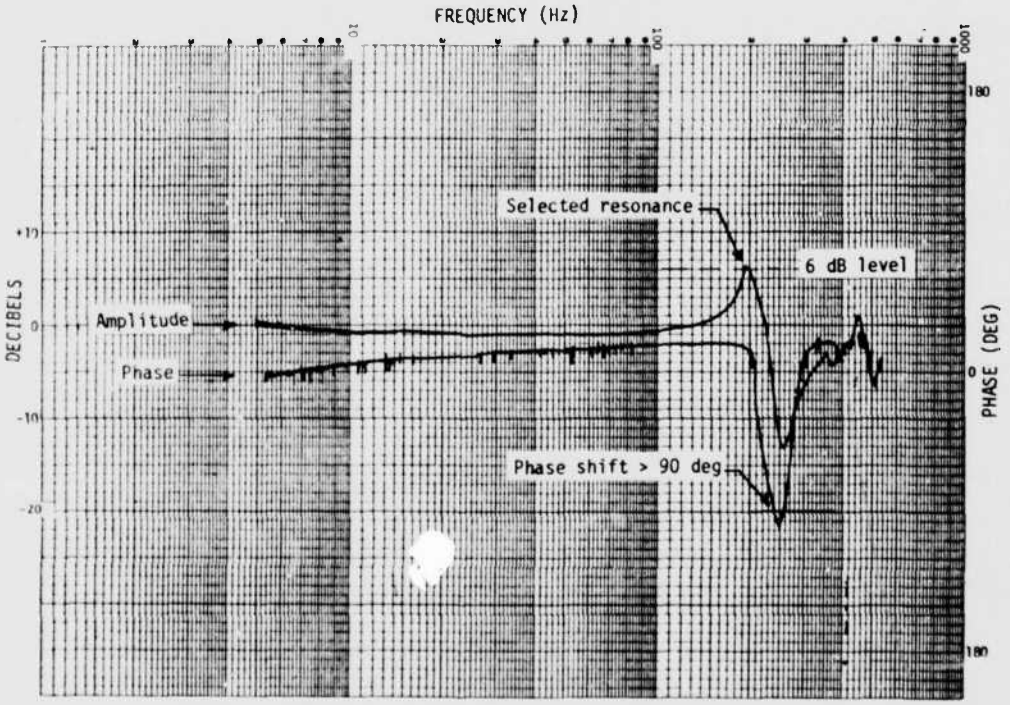


Figure C-32. Spectrum Analysis Plot, Inverter Lateral II Response/Control, Lateral II Axis Vibration, Full-Level Run, 14 September 1976

TABLE C-II

Common Module Resonances

Common Module	Axis	Resonance Found	Resonant Frequency (Hz)	g Level
Video Electronics (preamplifier)	Long	Yes (2)	225	14.0
			500	14.0
	Lat I	Yes	185	57.5
	Lat II	No	-	-
Video Electronics (postamplifier)	Long	Yes (2)	385	12.5
			500	14.0
	Lat I	Yes (2)	120	62.5
	Lat II	Yes	450	31.0
Mechanical Scanner	Long	No	-	-
	Lat I	No	-	-
	Lat II	Yes	496	22.0*
Scan and Interlace	Long	Yes (2)	313	12.5
			383	10.5
	Lat I	No	-	-
	Lat II	No	-	-
Cooler	Long	Yes	277	11.5
	Lat I	No	-	-
	Lat II	Yes	269	10.0
Inverter	Long	No	-	-
	Lat	Yes	480	33.0
	Lat II	Yes	198	10.5
IR Imager	Long	No	-	-
	Lat I	No	-	-
	Lat II	No	-	-
Visual Collimator	Long	No	-	-
	Lat I	No	-	-
	Lat II	No	-	-

*Resonant dwell not performed at 496 Hz per Martin-Marietta NVL agreement. Sine cycle test performed from 5 to 491 to 5 Hz. The 491 Hz is within allowable tolerance of 500±2 percent. No analyzer plot run was made.

C.4 Video Electronics Vibration Test Analysis

Vibration tests of the video electronics modules were performed from 9 through 19 August 1976 using the Environmental Laboratory's MB C-90 vibration exciter. The modules exposed to the vibration environment were: postamplifier SN 003, preamplifier SN 011, auxiliary control SN 001, and bias regulator SN 002.

Vibration exposure started with the low-level (1g) resonance search in the longitudinal axis on 11 August 1976. Resonant frequencies were recorded at 249, 325, 410, and 500 Hz. Upon beginning the first resonant dwell at full test levels, resonant frequencies were seen to vary greatly from those recorded during the low-level resonance search because of the higher g levels during dwell. A second resonance search was thus performed to determine the resonant frequencies, and consisted of a 15-minute full-level sine sweep from 5 to 500 to 5 Hz. Only three resonances were found during the full-level search; and their frequencies had shifted to 225, 385, and 500 Hz (as seen in Figures C-21 and C-22). It was decided to perform all final resonance searches at full level for all common modules. (The full level resonance searches were counted in the total sine cycling time as permitted in MIL-STD-810B.)

No further problems were encountered during longitudinal axis testing, and all channel output data were found to be acceptable. Total full level vibration times in the longitudinal axis are summarized as follows:

	Minutes
Full level resonance search	15
Resonance dwell at 225 Hz	30
Resonance dwell at 385 Hz	30
Resonance dwell at 500 Hz	30
Sine cycle testing	75
Total time (longitudinal axis)	3 hours

	Minutes, Seconds	
Full level resonance search	15	
Resonance dwell at 120 Hz	30	
Troubleshooting (192 Hz)	*23	20
Sine sweeps (5 to 500 Hz)	22	30
Sine sweeps (5 to 500 Hz)	* 2	
Resonance dwell at 185 Hz	30	
Troubleshooting at 182 Hz	* 2	30
Resonance dwell at 275 Hz	30	
Sine cycle testing	52	30
Total time (lateral I axis)	3 hours	

*Not counted toward 3-hour test time.

The video electronic modules were inspected upon completion of all vibration exposure. No damage was found. The modules then successfully passed postvibration functional tests, further confirming the ability of the video electronic modules to withstand the vibration environment.

C.5 Scan Mechanism Vibration Test Analysis

The EDT mechanical scanner and scan and interlace assembly were subjected to the vibration environment from 18 through 20 September 1976, using C-90 vibration exciter in the Environmental Laboratory. A review of the vibration resonance search data resulted in identifying the following resonances (Table C-II and Figure C-28):

Longitudinal axis - 12.5g at 313 Hz (scan card)
10.5g at 383 Hz (scan card)
Lateral II axis - 22.0g at 496 Hz (mechanical scanner)

No resonances were found in the lateral I axis. In the lateral II axis, sine cycle testing was performed from 5 to 491 to 5 Hz with NVL concurrence to avoid the resonance at 496 Hz. (Since the allowable frequency tolerance at 500 Hz is ± 2 percent, 491 Hz would still be within the allowable tolerance.)

Vibration testing was next performed in the lateral II axis (vibration parallel to the cards). The full-level resonance search revealed one resonance on the postamplifier card at a frequency of 450 Hz (shown in Figure C-23). Data taken during this phase of testing revealed no damage or out-of-tolerance condition. Total full-level test times in the lateral II axis were:

	Minutes
Full level resonance search	15
Resonance dwell at 450 Hz	30
Since cycle testing	135
Total time (lateral II axis)	3 hours

The last axis of testing was the lateral I axis (vibration perpendicular to cards). As expected, the more severe resonance conditions occurred in this axis. Resonances were initially found at 120, 190, and 365 Hz with amplitudes as high as 62.5g (Figures C-24 and C-25).

After completing the first resonance dwell test at 120 Hz, an evaluation was made using different rubber pad configurations for the test box cover. It was decided to use the original rubber pads covered with a layer of "missile" tape (Kendal P/N 231, PPT 60D, type 4 or equivalent). Because of this change, the full level resonance search was repeated with only two resonance at 275 Hz (Figures C-26 and C-27). Dwell tests at the above frequencies and the remainder of sine cycle testing were completed on 19 August 1976. Total lateral I axis vibration times were:

Longitudinal Axis	Hours, Minutes
Full level resonance search	15
Rerun full level resonance search	15
Resonance dwell at 313 Hz	30
Resonance dwell at 383 Hz	30
Sine cycle testing	1 30
Total time (longitudinal axis)	3 hours

Lateral I Axis	
Full level resonance search	15
Sine cycle tesing	2 45
Total Time (lateral I axis)	3 hours

Lateral II Axis	
Full level resonance search	15
Rerun full level resonance search	15
Sine cycle testing	2 30
Total time (lateral II axis	3 hours

An analysis of the functional test data compiled during and after vibration exposure and a post-test visual inspection revealed no anomalies, out-of-tolerance conditions, or structural damage as a result of exposing the mechanical scanner and scan and interlace assembly to the vibration environment. However, the resonance condition at 496 Hz mentioned at the beginning of this section could pose a problem since the scanner started chattering and the interlace transfer output became erratic at that frequency.

C.6 Vibration Test Analysis, Optical Modules

Vibration tests of the IR imager and visual collimator were carried out from 27 through 31 August 1976. The vibration environment was generated using the C-90 vibration exciter in the Environmental Laboratory.

An analysis of the resonance search records revealed that there were no resonances in any of the three test axes for either the IR imager or visual collimator. As a result, optical module vibration times in each

axis consisted of a 15-minute resonance search at full level followed by 2 hours and 45 minutes of sine-cycle testing.

No functional tests were performed while vibrating the optical modules. However, after completing the vibration exposure, visual inspections and functional tests of each module proved that the imager and collimator were unaffected by the vibration environment.

C.7 Cooler/Inverter Vibration Test Analysis

Vibration tests of the EDT cooler/inverter were performed in the Environmental Laboratory from 13 through 15 September 1976 using the C-90 vibration exciter.

An analysis of the resonance search data taken during vibration testing resulted in identifying the following resonances (Table C-II and Figures C-29 thru C-32):

Longitudinal axis - 11.5g at 277 Hz (cooler)
Lateral I axis - 33.0g at 480 Hz (inverter)
Lateral II axis - 10.5g at 198 Hz (inverter)
10.0g at 269 Hz (cooler)

Total vibration time in each axis is identified below:

Longitudinal Axis	Hours, Minutes
Full level resonance search	15
Resonance dwell at 277 Hz	30
Sine cycle test	2 15
Total time (longitudinal axis)	3 hours

Lateral I Axis	
Full level resonance search	15
Resonance dwell at 480 Hz	30
Sine cycle test	2 15
Total time (lateral I axis)	3 hours

Lateral II Axis

Full level resonance search		15
Resonance dwell at 198 Hz		30
Resonance dwell at 269 Hz		30
Sine cycle test	1	45
Total time (lateral II axis	3 hours	

At completion of the vibration exposure, visual examinations and functional tests revealed no damage or out-of-tolerance conditions, indicating that the cooler/inverter design is capable of successfully operating in the stated vibration environment.

APPENDIX D

COMMON MODULE ELECTROMAGNETIC INTERFERENCE TEST REPORT

The material in this appendix is provided through the courtesy of Magnavox who conducted the subject test and compiled the results in Volume I of Electro-Optical Systems Report No. 222, the title page of which is reproduced below. For further information on this report, please query the Night Vision Laboratory, AMSEL-NV-SD, Fort Belvoir, Virginia 22060.

VOLUME I

TEST REPORT

ELECTROMAGNETIC INTERFERENCE TESTS
OF
COMMON MODULES

PREPARED FOR:

DEPARTMENT OF THE ARMY
UNITED STATES ARMY ELECTRONICS COMMAND
NIGHT VISION LABORATORY
FORT BELVOIR, VIRGINIA 22060

CONTRACT NO. DAAG53-75-C-0178

CDRL No. A023

APPROVED BY:

T. J. Corbett
Project Manager,
Common Modules

APPROVED BY:

R. F. Anderson
Program Manager
FLIR Programs

Magnavox
GOVERNMENT & INDUSTRIAL ELECTRONICS COMPANY
ADVANCED PRODUCTS DIVISION ELECTRO-OPTICAL SYSTEMS
46 INDUSTRIAL AVENUE MAHWAH, N.J. 07430

EOSR No. 222

10 October 1977

1. INTRODUCTION

1.1 Purpose and Scope

This report describes results of electromagnetic interference (EMI) tests of nine common modules, manufactured by Magnavox Government and Industrial Electronics Co., Mahwah, NJ. Tests were performed in accordance with applicable requirements of Notice 4, MIL-STD-461A and Notice 3, MIL-STD-462, as specified in the Magnavox test plan. The following test methods were performed: CE01, CE03, CE04, CE05, RE02, CS01, CS02 and RS03.

1.2 Applicable Documents

MIL-STD-461A	Electromagnetic Interference Characteristics, Requirements for Equipment, dated 1 August 1968, with Notice 4 dated 9 February 1971.
MIL-STD-462	Electromagnetic Interference Characteristics, Measurement of, dated 31 July 1967, with Notice 3 dated 9 February 1971.
Test Plan	Magnavox Common Module EMI Test Plan, dated January 1977, revised February 1977.

2. TEST SAMPLE

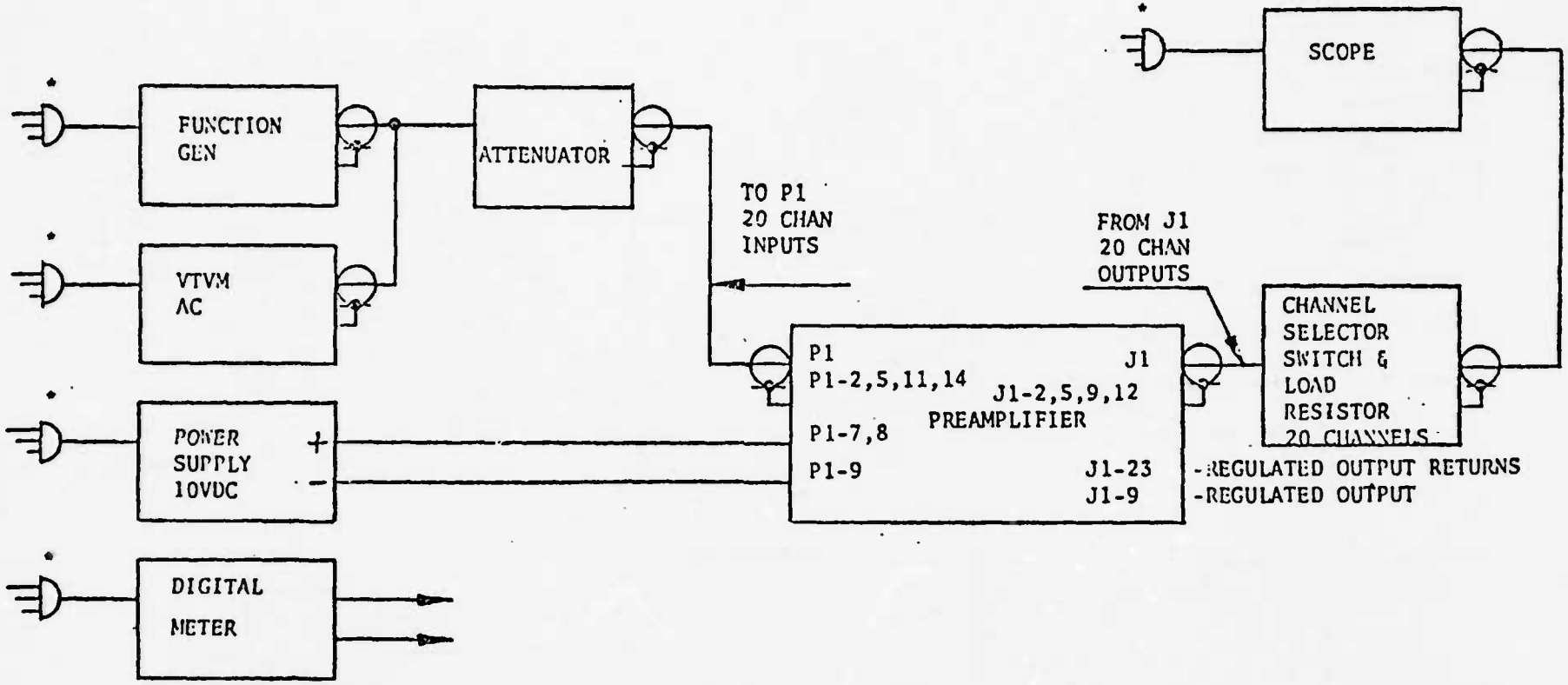
2.1 Setup and Operation

Each module under test was set up on a copper-covered test bench inside the shielded enclosure described in Section 4.1. It was located 10 $\pm$ 2 cm from the front edge of the ground plane. Leads and cables were located, where practical, within 10 $\pm$ 2 cm of the front edge of the ground plane and raised 5 cm above it on insulated supports. Detailed test setups of individual modules are shown in Figures 1 through 8.

The modules were operated in HI POWER mode for emission tests, and in HI or LO POWER mode for susceptibility tests, depending on the module under test. Prior to performance of EMI tests, each module was checked for normal operation by the Magnavox representative.

2.2 Determination of Susceptibility

While the various susceptibility test signals were applied, each module was monitored for any indications of malfunction or degradation in performance which would indicate susceptibility. Specific monitor points and susceptibility criteria are listed in Table I.



D-3

* CONNECT TO 115 VAC

FIGURE 1 PREAMPLIFIER TEST SETUP

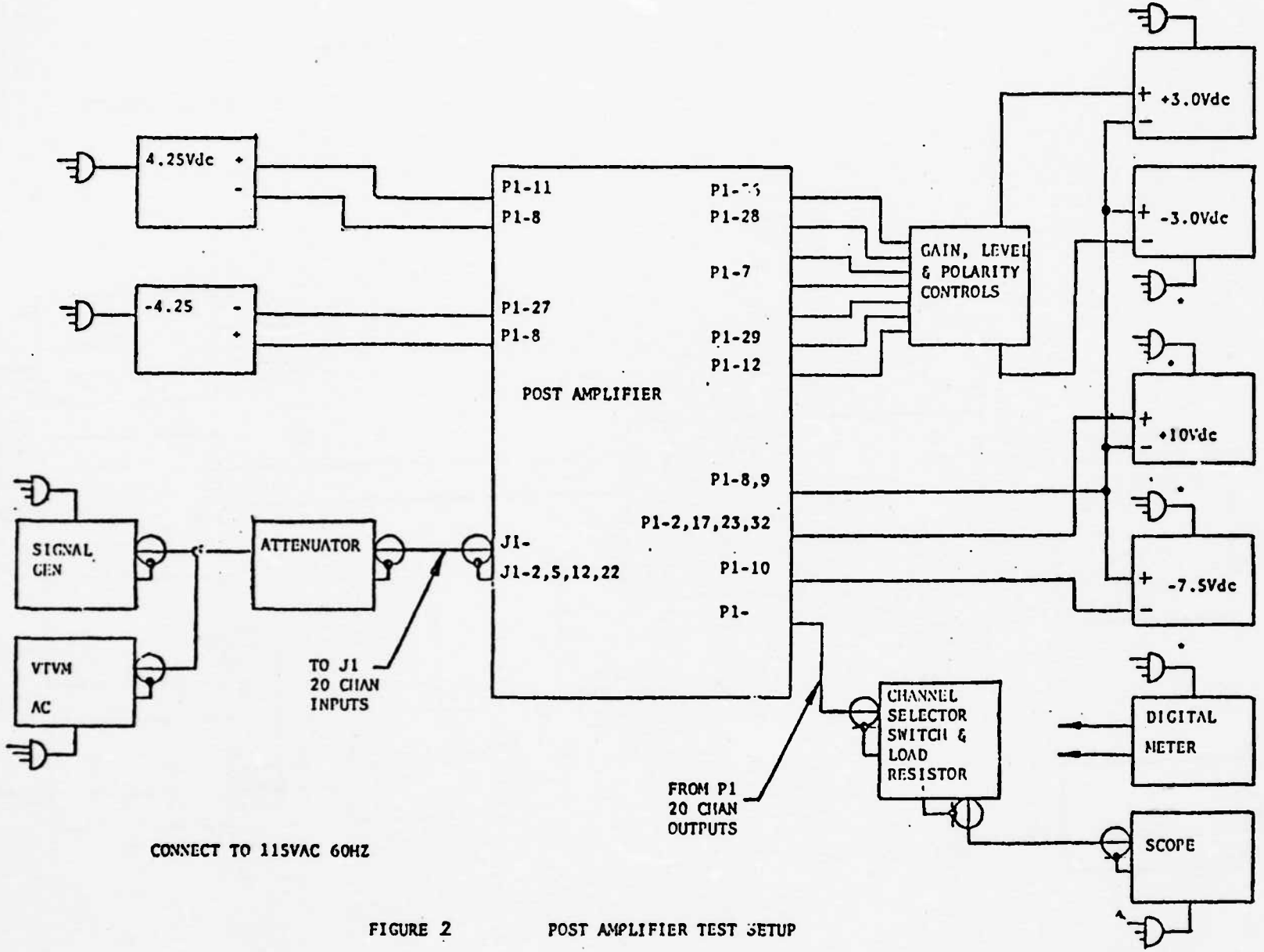
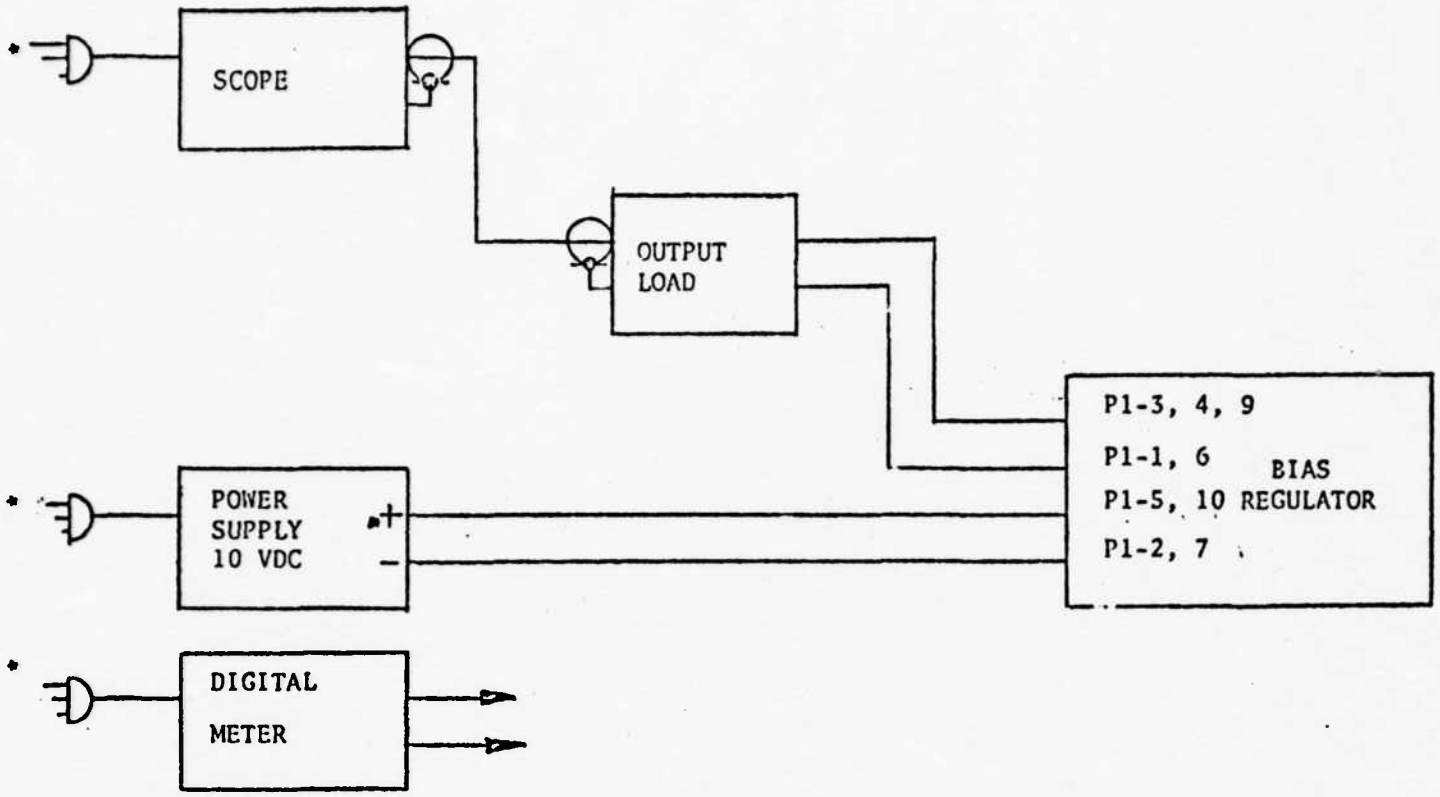


FIGURE 2 POST AMPLIFIER TEST SETUP



* CONNECT TO 115 VAC 60HZ

FIGURE 4 BIAS REGULATOR TEST SETUP

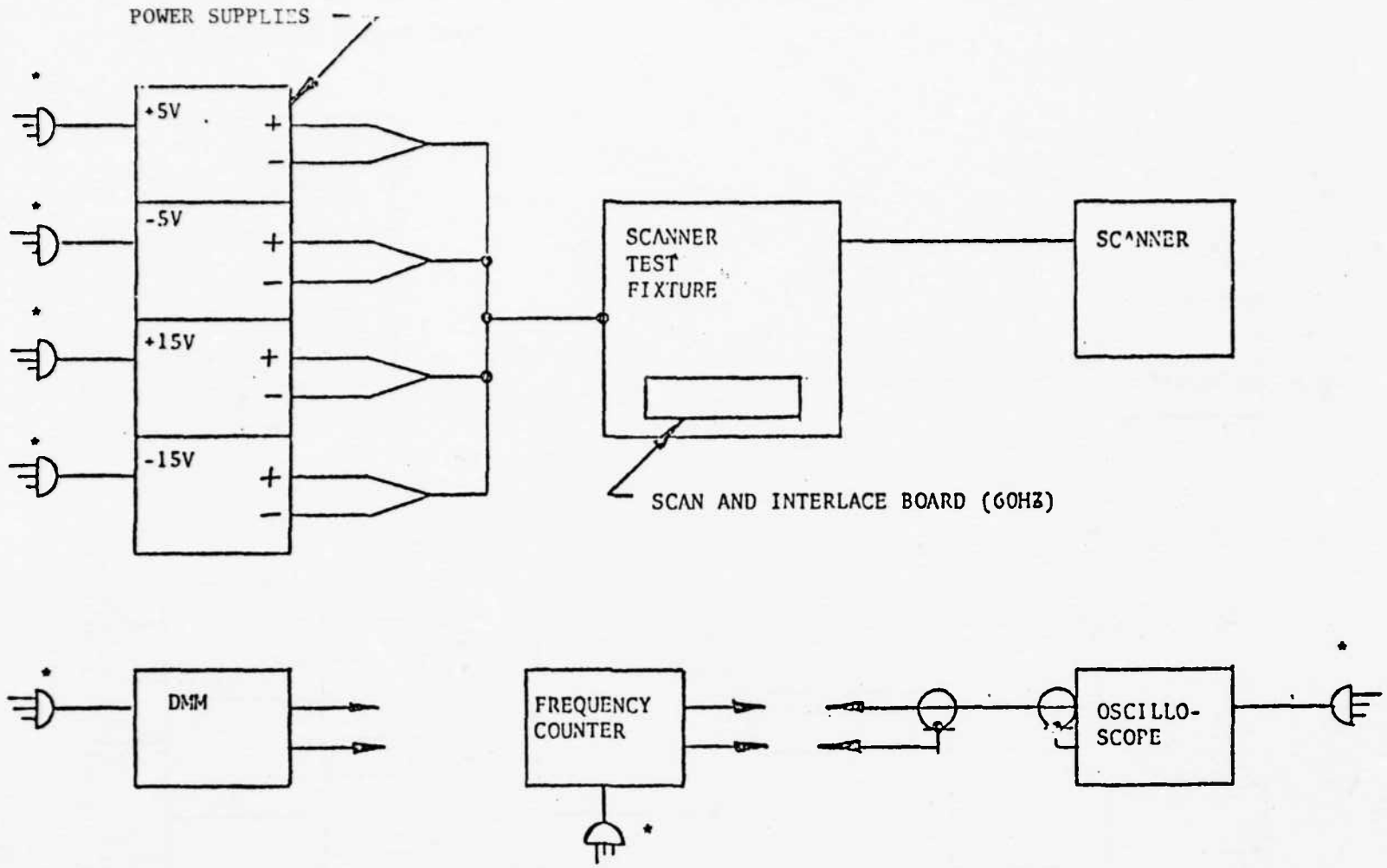
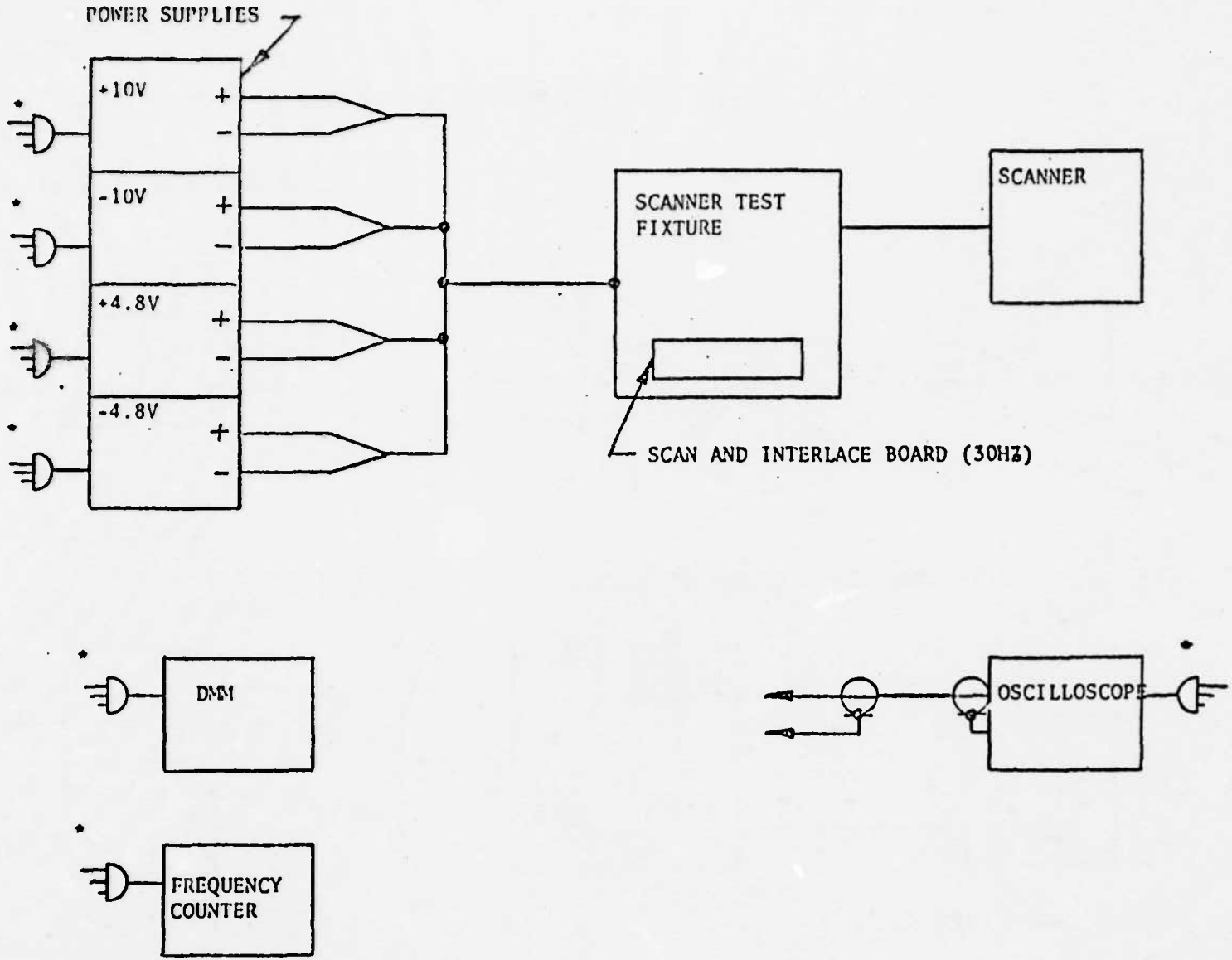
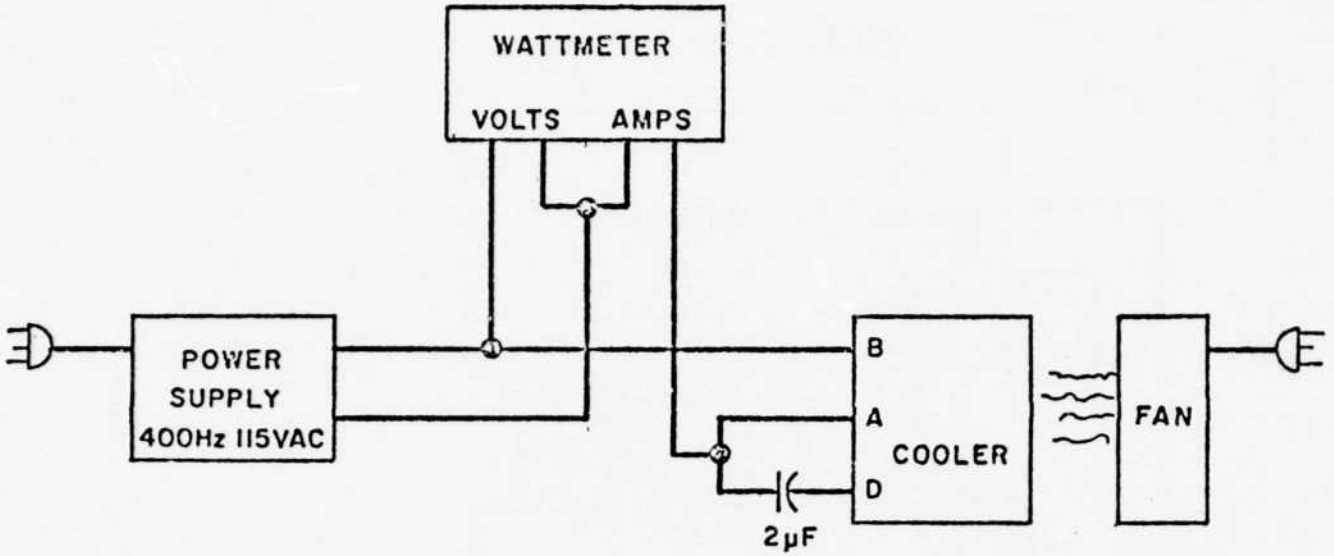


FIGURE 5 SCANNER AND SCAN AND INTERLACE BOARD (60HZ) TEST SETUP



* CONNECT TO 115VAC 60HZ.

FIGURE 6 SCANNER AND SCAN AND INTERLACE BOARD (30HZ, LOW POWER) TEST SETUP



COOLER TEST SETUP

FIGURE 7 COOLER TEST SETUP

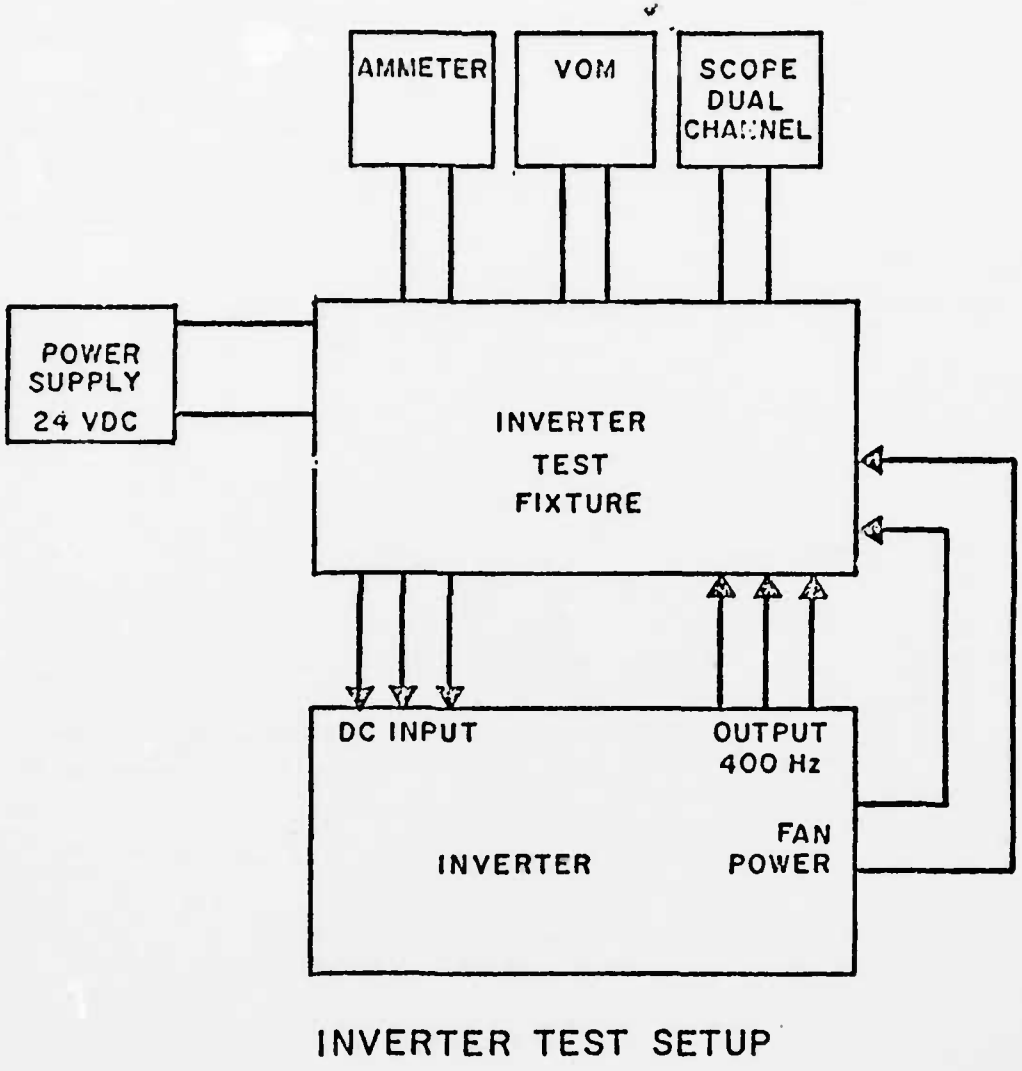


FIGURE 8 INVERTER TEST SETUP

TABLE 1 - SUSCEPTIBILITY MONITOR POINTS AND CRITERIA

MODULE	MONITOR POINTS	SUSCEPTIBILITY CRITERIA
Preamplifier	CH 18 output ripple.	Ripple exceeds 2.8 microvolts.
Post Amplifier	CH 1 output ripple.	Ripple exceeds ± 100 millivolts when signal applied to + 10 V input, or ± 50 mV when applied to -7.5 V input, or ± 0.2 mV when applied to ± 4.25 V input.
Auxiliary Control	Post Amplifier CH 1 output ripple.	Ripple exceeds 100 millivolts.
Bias Regulator	Output voltage ripple.	Ripple exceeds 2 millivolts.
Scanner and Scan and Interlace Board (60 Hz)	Scan and Interlace waveforms.	Distortion of waveforms, FM or AM of waveforms.
Scan and Interlace Board (30 Hz)	Scan/Tach and Interlace waveforms.	Distortion of waveforms, FM or AM of waveforms.
DC/AC Inverter	AC output voltage and ripple.	Change in output voltage or measurable ripple.
Cooler	Performance.	Degradation in performance.

3. EMISSION AND SUSCEPTIBILITY SIGNAL LEVEL LIMITS

The following interference limits were applied during the tests:

METHOD	DESCRIPTION	REFERENCE IN TEST PLAN
CE01	Conducted, 30 Hz - 50 kHz, DC Power Lines	Figure 4
CE03	Conducted, 30 Hz - 50 kHz, Control and Signal Lines	Figure 4
CE04	Conducted, 50 kHz - 50 MHz, Power Lines	Figures 11 and 12
CE05	Conducted, 50 kHz - 50 MHz, Control and Signal Lines	Figures 11 and 12
RE02	Radiated, 14 kHz - 10 GHz, Electric Field	Figures 19 and 20

The following susceptibility signal level limits were applied:

METHOD	DESCRIPTION	REFERENCE IN TEST PLAN
CS01	Conducted, 30 Hz - 50 kHz, DC Power Lines	Figure 15
CS02	Conducted, 50 kHz - 400 MHz, Power Lines	Figure 17
RS03	Radiated, 14 kHz - 10 GHz, Electric Fields	Section 5.8.5

4. TEST FACILITIES

4.1 Test Site

The tests were performed in an armored plywood shielded enclosure with dimensions of 20 feet by 14 feet by 8 feet high. Shielding effectiveness to electric fields and plane waves exceeded 80 dB from 14 kHz to 10 GHz, measured in accordance with MIL-STD-285. All power lines were filtered with filters which provided at least 80 dB

of attenuation above 10 kHz, measured in accordance with MIL-STD-220A. Ambient levels were below limits and were verified during the tests.

The copper ground plane, on which the test sample was mounted had dimensions of 3 feet by 8 feet and a thickness which exceeded 0.25 mm. Bonds to the shielded enclosure wall were no more than 90 cm apart. Bonding resistance was less than 2.5 milliohms.

Signal lines between test equipment outside the enclosure and antennas and other equipment inside the enclosure penetrated the enclosure wall via coaxial feedthrough connectors. These connectors provided a continuous, low-impedance path for the signals.

4.2 Test Personnel

AEL Project Supervisor:	Margaretta Stone
AEL EMI Test Supervisor:	Eugene Barber
AEL EMI Test Technician:	Jack Arroyo-Perez
Magnavox Representative:	Bill Hennig

4.3 Test Equipment

Table 2 contains a list of AEL equipment used in the tests. All equipment was calibrated prior to use, at the Instrument Calibration Laboratory, American Electronic Laboratories, Inc., Colmar, Pennsylvania. Calibration was performed in accordance with MIL-C-45662A, using standards traceable to the National Bureau of Standards (NBS) and checked on a routine basis as recommended in NBS Circular 578.

4.4 Measurement Accuracy

Measurement accuracy complied with applicable requirements of Section 5.8, MIL-STD-461A. Amplitude accuracy was $\pm$ 2 dB and frequency accuracy was $\pm$ 2 per cent.

5. SUMMARY OF TEST PROCEDURES

Test procedures complied with applicable requirements of MIL-STD-461A with Notice 3, as modified by the Magnavox test plan. Detailed procedures are discussed in the appendices covering each test.

6. SUMMARY OF TEST RESULTS

Detailed test results are described in the appendices covering each test, and summarized in Table 3.

TABLE 2 - AEL TEST EQUIPMENT

NOMENCLATURE/ FREQUENCY	MANUFACTURER	MODEL NO.	SERIAL NO.	CALIBRATION DUE DATE
Signal Sources:				
5 Hz - 600 kHz	Hewlett-Packard	200CD	4621	5 Nov. 1977
10 kHz - 50 MHz	Winslow	URM-25D	3062	4 Nov. 1977
50 kHz - 65 MHz	Hewlett-Packard	606B	7764	18 Aug. 1977
10 MHz - 480 MHz	Hewlett-Packard	608D	6773	15 Oct. 1977
50 MHz - 1 GHz	Microdot	M455	7471	11 Aug. 1977
450 MHz - 1.23 GHz	Hewlett-Packard	612A	2262	24 Sept. 1977
0.8 GHz - 2.4 GHz	Hewlett-Packard	614A	7737	1 Oct. 1977
1.8 GHz - 4.0 GHz	Hewlett-Packard	616B	5862	14 Sept. 1977
3.8 GHz - 7.6 GHz	Hewlett-Packard	618C	5889	11 Aug. 1977
7 GHz - 11 GHz	Hewlett-Packard	620A	7736	2 Sept. 1977
Amplifiers:				
30 Hz - 150 kHz	Solar	6552-1A	7447	N/A
14 kHz - 25 MHz	Honeywell	AW-204	6762	2 Aug. 1977
10 kHz - 220 MHz	IFI	M402/M5000	9438	N/A
10 kHz - 25 MHz	AEL	120B	7912	24 July 1977
1 GHz - 2 GHz	AEL	T607	3862	8 Nov. 1977
2 GHz - 4 GHz	AEL	T608	3103	8 Nov. 1977
2 GHz - 4 GHz	Hewlett-Packard	491C	5482	27 Nov. 1977
4 GHz - 8 GHz	AEL	T609	3102	17 Dec. 1977
4 GHz - 8 GHz	Alfred	5030	5839	25 Aug. 1977
7 GHz - 12.4 GHz	AEL	T610	3104	18 Oct. 1977
Receivers:				
30 Hz - 50 kHz	Fairchild	EMC-10	6552	2 Sept. 1977
14 kHz - 1 GHz	Singer	NF-105	1418	7 July 1977
1 GHz - 10 GHz	Singer	EMA-910	6483	2 Sept. 1977
Spectrum Analyzer:				
Display	Hewlett-Packard	141T	9203A	6 May 1978
IF Head	Hewlett-Packard	8552B	9203B	6 May 1978
1 kHz - 110 MHz	Hewlett-Packard	8553B	9203C	6 May 1978
10 MHz - 40 GHz	Hewlett-Packard	8555A	8458D	13 Apr. 1978
Current Probes:				
10 Hz - 50 kHz	Fairchild	PCL-10	7346	N/A
30 Hz - 50 MHz	Singer	CP-105	6747	N/A
10 kHz - 100 MHz	Stoddart	91550-2	465	N/A
LISN's:				
10 kHz - 10 MHz	Honeywell	3861	6786	12 Nov. 1977
			6787	12 Nov. 1977
150 kHz - 1 GHz	Stoddart	91221-1	6625	11 Nov. 1977
			6626	11 Nov. 1977

TABLE 2 - AEL TEST EQUIPMENT (CONT.)

NOMENCLATURE/ FREQUENCY	MANUFACTURER	MODEL NO.	SERIAL NO.	CALIBRATION DUE DATE
Antennas:				
10 kHz - 25 MHz	AEL	P/O 120B	None	N/A
14 kHz - 25 MHz	Honeywell	P/O AW204	None	N/A
14 kHz - 220 MHz	IFI	EFG-2	9438C	N/A
150 kHz - 30 MHz	Singer	VA-105	732	N/A
20 MHz - 200 MHz	White	407A	6802	N/A
200 MHz - 1 GHz	EMCO	CLP-1A	7794,7797	N/A
1 GHz - 10 GHz	EMCO	CLP-1B	7793,7796	N/A
Attenuators:				
DC - 1 GHz	Kay	30-0	4789	15 Dec. 1977
DC - 18 GHz	Hewlett-Packard	8495B	10247	8 Sept. 1977
Other Equipment:				
Field Sensor	IFI	EFS-1	9438A	20 July 1977
Voltmeter	Hewlett-Packard	400F	6311	30 Sept. 1977
10 uF Feedthrough Capacitor	Solar	6512-106R	None	N/A
Transformer, Audio	Solar	6220-1A	None	N/A
Transformer, Isolation	Emtech	M5469	None	N/A

TABLE 3 - SUMMARY OF TEST RESULTS

MODULE	TEST	SUMMARY OF RESULTS
Preamplifier	CE01	Passed.
	CE03	Passed.
	CE04	Passed.
	CE05	Passed.
	RE02	Passed.
	CS01	Susceptible to signals, applied to + 10V lead, with levels of 10 - 12 mV, in range of 30 Hz to 50 kHz.
	CS02	Susceptible to signals, applied to + 10V lead, with levels 3 - 58 dB below required level, in range of 50 kHz to 10 MHz.
	RS03	Susceptible to signal levels of 0.25 V/M to 6.3 V/M, at frequencies of 2 - 60 MHz, 80 - 225 MHz and 300 - 600 MHz.
Post Amplifier	CE01	Passed.
	CE03	Passed.
	CE04	Passed.
	CE05	Passed.
	RE02	Passed.
	CS01	Susceptible to signals, applied to + 10V lead, with levels of 4 - 500 mV, in range of 30 Hz to 50 kHz. Susceptible to signals, applied to - 7.5V lead, with levels of 75 - 750 mV, in range of 30 Hz to 50 kHz. Susceptible to signals, applied to + 4.25V lead, with levels of 0.65 - 0.80 mV, in range of 30 Hz to 50 kHz. Susceptible to signals, applied to - 4.25V lead, with levels of 0.8 - 1.0 mV, in range of 30 Hz to 50 kHz.
	CS02	Susceptible to signals, applied to + 4.25V lead, with levels 0 - 40 dB below required level, in range of 50 kHz to 1 MHz. Susceptible to signals, applied to - 4.25V lead, with levels 0 - 28 dB below required level, in range of 50 kHz to 800 kHz.
	RS03	Susceptible to signal levels of 0.1 V/M to 4 V/M, at frequencies of 4.9 - 16 MHz and 18 MHz to 1 GHz.
Auxillary Control	CE01	Passed.
	CE03	Passed.
	CE04	Passed.
	CE05	Emission from IR Level/Gate Out line exceeded limit by 8 dB maximum, in range of 1.2 - 2.7 MHz.

TABLE 3 - SUMMARY OF TEST RESULTS (CONT.)

MODULE	TEST	SUMMARY OF RESULTS
Auxiliary Control (Cont.)	RE02	Passed.
	CS01	Susceptible to signals, applied to + 10V lead, with levels of 2 - 250 mV, in range of 30 Hz to 50 kHz. Susceptible to signals, applied to - 7.5V lead, with levels of 3 - 50 mV, in range of 30 Hz to 50 kHz.
	CS02	Susceptible to signals, applied to + 10V lead, with levels 2 - 7 dB below required level, in range of 50 kHz to 300 kHz.
	RS03	Susceptible to signal levels of 0.5 V/M to 9 V/M, at frequencies of 19.7 - 23 MHz, 26.2 - 190 MHz, 220 MHz and 900 MHz.
Bias Regulator	CE01	Passed.
	CE03	Test not required.
	CE04	Passed.
	CE05	Test not required.
	RE02	Passed.
	CS01	Susceptible to signals, applied to the + 10V lead, with levels of 1.65 - 480 mV, in range of 30 Hz to 50 kHz.
	CS02	Passed.
	RS03	Susceptible to signal levels of 0.1 V/M to 7.5 V/M, at frequencies of 106 kHz to 130 MHz and 180 - 225 MHz.
Scanner	CE01	Passed.
	CE03	Tested with Scan Interlace Board (60 Hz).
	CE04	Passed.
	CE05	Tested with Scan Interlace Board (60 Hz).
	RE02	Emission exceeded limits by 12 dB maximum, in range of 14 kHz to 43 kHz.
	CS01	Susceptible to signals, applied to + 15V lead, with levels of 0.8 - 1.0 V, in range of 30 Hz to 4 kHz. Susceptible to signals, applied to - 15V lead, with level of 1.0 volt, in range of 30 Hz to 4 kHz.
	CS02	Passed.
	RS03	Susceptible to signal levels of 1 V/M to 8 V/M, at frequencies of 13.2 - 56 MHz, 80 - 85 MHz, 100 MHz, 130 MHz and 500 MHz.

TABLE 3 - SUMMARY OF TEST RESULTS (CONT.)

MODULE	TEST	SUMMARY OF RESULTS
Scan and Interlace Board (60 Hz)	CE01	Passed.
	CE03	Emission on Sync Return line exceeded limit by 25 dB maximum, in range of 30 Hz to 82 Hz. Emission on Interlace Position LO line exceeded limit by 23 dB maximum, in range of 30 Hz to 80 Hz.
	CE04	Emission on + 5V input line exceeded limit by 4 dB maximum, in range of 85 kHz to 160 kHz.
	CE05	Passed.
	RE02	Emission exceeded limits by 25 dB maximum, in range of 14 kHz to 50 kHz.
	CS01	Susceptible to signals, applied to the + 5V lead, with levels of 50 - 300 mV, in range of 60 Hz - 50 kHz. Susceptible to signals, applied to - 5V lead, with levels of 25 - 100 mV, in range of 50 Hz to 50 kHz. Susceptible to signals, applied to + 15V lead, with levels of 55 - 500 mV, in range of 30 Hz to 50 kHz. Susceptible to signals, applied to - 15V lead, with levels of 50 - 500 mV, in range of 30 Hz to 50 kHz.
	CS02	Passed.
	RS03	Susceptible to signal levels of 1 V/M to 8 V/M, at frequencies of 12.96 - 15.6 MHz, 31.4 - 800 MHz and 1 GHz.
Scan and Interlace Board (30 Hz)	CE01	Passed.
	CE03	Passed.
	CE04	Emission from - 4.8V line exceeded limits by 7 dB maximum from 1.4 MHz to 2.1 MHz. Emission from + 10V line exceeded limits by 11 dB maximum from 1.3 MHz to 2.2 MHz. Emission from - 10V line exceeded limits by 11 dB maximum from 1.3 MHz to 2.2 MHz. Emission from DC Return line exceeded limits by 12 dB maximum from 1.3 MHz to 2.2 MHz.
	CE05	Emission from Chassis Ground line exceeded limits by 7 dB maximum from 2.9 MHz to 3.2 MHz. Emission from Phase Select line exceeded limits by 3 dB maximum from 7.8 MHz to 8.4 MHz.

TABLE 3 - SUMMARY OF TEST RESULTS (CONT.)

MODULE	TEST	SUMMARY OF RESULTS
Scan and Interlace Board (30 Hz)	RE02	Passed.
	CS01	Passed.
	CS02	Passed.
	RS03	Susceptible to signal levels of 0.1 V/M to 6.5 V/M, at frequencies of 2 - 150 MHz, 170 MHz and 200 - 900 MHz.
DC/AC Inverter	CE01	Emission from DC Return line exceeded limits by 4 dB maximum from 19 kHz to 32 kHz.
	CE03	Passed.
	CE04	Passed.
	CE05	Passed.
	RE02	Passed.
	CS01	Susceptible to signals, applied to + 28V lead, with levels of 47 - 255 mV, in range of 30 - 50 kHz.
	CS02	Passed.
	RS03	Passed.
Cooler	CE01	Test not required.
	CE03	Test not required.
	CE04	Passed.
	CE05	Test not required.
	RE02	Passed.
	CS01	Test not required.
	CS02	Passed.
	RS03	Passed.

APPENDIX E

RATCHES' MODEL FOR FLIR SYSTEM PERFORMANCE

The expression for MRT in the horizontal scan direction is:

$$MRT_H = SNR \cdot \frac{\pi^2}{4\sqrt{14}} \cdot \frac{NE\Delta T}{MTF_H} \cdot \left(\frac{\Delta Y \cdot v \cdot Q \cdot \nu_T}{\Delta f_n \cdot F_r \cdot t_e \cdot \eta_o} \right)^{1/2} \qquad \text{(E-1)}$$

where

SNR = signal-to-noise ratio required to resolve four-bar target
= 2.25.

$NE\Delta T$ = system noise equivalent temperature difference (°C)

MTF_H = system horizontal (i.e., scan direction) modulation transfer function from input optics through the observer's eye

ΔY = detector vertical angular subtense in object space (mrad)

v = scanner angular rate in object space (mrad/s)

F_r = system frame rate (20 to 62 frame/s)

t_e = eye integration time (0.2 second)

While t_e is nominally 0.2 second, it can be used to account for the display overlap produced by the inequality of detector and LED vertical angular subtenses (in object space) by the relation:

$$t_e = 0.2 \cdot l_v/L \qquad \text{(E-2)}$$

where

l_v = LED element height

L = LED element center-to-center spacing

η_o = system overscan ratio (nominally 1.0 for the modular imaging system)

Q = system noise equivalent combined electrical and spatial bandwidth in line pairs per mrad (lp/mrad)

Δf_n = system combined detector and electronics noise equivalent bandwidth (Hz):

$$\Delta f_n = \int_0^\infty S_n(f)\, H_{elec}^2(f)\, df.$$

This definition for Δf_n differs from that given in the NVL report* in that it includes both detector and electronics contributions to the system noise power spectrum. Furthermore, it does not contain terms relating to aperture correction or additional electronic filtering because the electronic modules contain no internal provision for these features. Here:

$S_n(f)$ = system normalized noise power spectrum referenced to preamplifier input including detector and electronics sources.

f = temporal frequency (Hz)

H_{elec} = electronics MTF (Appendix B, Figure B-2)

ν_T = target bar pattern fundamental frequency (lp/mrad).

The above quantities from equation (E-1) are further expressed as a function of parameters that either characterize the common modules or are system dependent:

$$NE\Delta T = (NE\Delta T_{det}^{\ 2} + NE\Delta T_{elec}^{\ 2})^{1/2} \qquad \text{(E-3)}$$

(This $NE\Delta T$ is defined by a more general expression than those appearing in the Ratches' model and elsewhere. It includes electronics noise defined over the broad noise bandwidth, Δf_n).

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* J. Ratches, et al, "Night Vision Laboratory Static Performance Model for Thermal Viewing System," Research and Development Technical Report ECOM-7043, April 1975.

$NE\Delta T_{det}$ = $NE\Delta T$ from detector noise sources and background to the extent background is included in D^*, or

$$NE\Delta T_{det} = \pi \cdot \frac{4 \cdot F\#^2 \cdot \sqrt{\Delta f_d}}{\sqrt{A_d} \cdot To \cdot Ta \int_{\Delta\lambda} D^*_\lambda \cdot \eta'_\lambda \cdot d\lambda} \qquad \text{(E-4)}$$

where

$F\#$ = IR optics f number

A_d = detector (element) active area (cm^2)

Ta = atmospheric transmittance (Ta = 1.0 for laboratory test environment)

To = IR optics transmittance (assumed constant over system spectral bandpass)

$T_o = T_T \cdot T_S \cdot T_I$

T_T = afocal telescope transmittance

T_S = IR scan mirror reflectivity

T_I = IR imaging optics transmittance

(Note that transmittance of detector window is deliberately omitted because it is assumed to be included in the D* measurement.)

$$\Delta f_d = \int_o^\infty S_d(f)\, H^2_{elec}(f)\, df \qquad \text{(E-5)}$$

$S_d(f)$ = detector normalized noise power spectrum at preamp input:

$$S_d(f) = \frac{S_D(f)}{S_D(f_o)}$$

where

$S_D(f)$ = detector noise power spectrum

$f_o = \nu_T / v.$

The wavelength integral over the system spectral bandpass, $\Delta\lambda$, in the NEΔT equation need not be computed in the expression because detector module detectivity, D^*, is specified in terms of peak detectivity, D^*_p, rather than a spectral response curve, D^*_λ. By defining a normalized detector spectral response $D_\lambda = D^*_\lambda / D^*_p$, the specified detectivity, D^*_p, may be moved outside the integral, as

$$\int_{\Delta\lambda} D^*_\lambda \cdot \eta'_\lambda \cdot d_\lambda = D^*_p \cdot \int_{\Delta\lambda} D_\lambda \cdot \eta'_\lambda \cdot d_\lambda$$

where η'_λ equals the temperature derivative of the Planck radiation equation. For a 300°K blackbody and typical HgCdTe spectral response characteristics:

$$\int_{7.5\ \mu m}^{12.0\ \mu m} D_\lambda \cdot \eta'_\lambda \cdot d_\lambda = 5.59 \times 10^{-5}\ W \cdot cm^{-2} \cdot sr^{-1} \cdot {}^\circ C^{-1}$$

and

$$\int_{\Delta\lambda} D^*_\lambda\ \eta'_\lambda\ d_\lambda = 5.59 \times 10^{-5}\ D^*_p. \qquad \text{(E-6)}$$

Further describing the terms in Equation (E-1):

$$Q = \int_o^\infty S_n(\nu) \cdot H_{N_H}{}^2(\nu) \cdot H_W{}^2(\nu) \cdot H_{EYE}{}^2(\nu) \cdot d\nu \qquad \text{(E-7)}$$

where

ν = object space frequency (lp/mrad)

= f (Hz)/v(mrad/s)

$S_n(\nu)$ = normalized combined detector and electronics noise power spectrum, $S_n(f)$, expressed as a function of spatial frequency (dimensionless)

$S_n(\nu)$ = 1 for system with flat noise spectrum

= $1.0 + \frac{500}{\nu \cdot \nu}$ for system with 1/f noise but otherwise characterized by flat noise spectrum (E-8)

= actual system normalized noise power spectrum including detector, modules, and system unique contributors when none of the above apply

H_{N_H} = noise filter function (MTF) from the electronics to the display, inclusive

$H_{N_H} = H_{elec} \cdot H_{LED} \cdot H_{VC} \cdot H_{eye}$ where terms are defined later (E-9)

H_{EYE} = observer's eye MTF

$$H_W = \frac{\sin(\pi\nu/2\nu_T)}{(\pi\nu/2\nu_T)} \cdot \quad \text{(E-10)}$$

In the MRT expression, the system MTF is defined as:

$$MTF_H = H_{LOS} \cdot H_{IR} \cdot H_{det} \cdot H_{elec} \cdot H_{LED} \cdot H_{VC} \cdot H_{eye} \quad \text{(E-11)}$$

where

H_{LOS} = stabilization MTF

H_{IR} = IR optics (combined afocal, scanner module, and IR imager module) MTF

H_{elec} = electronics MTF (Appendix B, Figure B-2)

H_{det} = detector spatial MTF

$$= \frac{\sin(\pi \cdot \Delta X \cdot \nu)}{(\pi \cdot \Delta X \cdot \nu)} \quad \text{(E-12)}$$

where

ΔX = detector horizontal angular subtense in object space (mrad)

$$= (d_h/F_e) \times 10^3 \quad \text{(E-13)}$$

where

d_h = detector horizontal dimension (inches)

F_e = IR optics effective focal length (inches)

H_{LED} = LED spatial MTF

$$= \sin \frac{(\pi \cdot \beta \cdot \nu)}{\pi \cdot \beta \cdot \nu} \qquad \text{(E-14)}$$

β = LED horizontal angular subtense in object space (mrad)

H_{vc} = visual channel MTF (including visual collimator, scanner, phase shift lens and, if used, image intensifier, eyepiece, cathode ray tube, etc., up to the observer's eye).

Finally, the detector vertical subtense in Equation (E-1) is defined as:

$$\Delta Y = (d_v/F_e) \times 10^3 \qquad \text{(E-15)}$$

where

d_v = detector vertical dimension (inches).

The above expressions will permit evaluation of system performance for a detector and background noise-limited system. However, the electronics contribution to total noise level should be considered for an accurate prediction of system performance. For instance, the representative system noise budget in paragraph 3.1.4 shows a total electronics root-mean-square (rms) noise level of 1.0 μV with the system 97.6 kHz bandwidth. (See bandwidth discussion in Appendix B.) This noise level is to be compared with the nominal detector (including ~75-degree cone background) rms noise level of:

$$N_D = \frac{R\ (V/W) \cdot [A_d\ (cm^2)]^{1/2} \cdot \Delta f_d^{1/2}}{D^*\ (cm\text{-}Hz^{1/2}/W)} \qquad \text{(E-16)}$$

$$= \frac{1.4 \times 10^4\ V/W \cdot (2.58 \times 10^{-5}\ cm^2)^{1/2} \cdot (81.2 \times 10^3\ Hz)^{1/2}}{2.4 \times 10^{10}\ cm\text{-}Hz^{1/2}/W}$$

$$= 0.84\ \mu V.$$

This noise level results if the minimum average values for detector responsivity, R, and D^* are used as given in the detector development specification. Measurements on detector modules show that actual noise levels range up to approximately 1.7 μV with both higher responsivity and D^*. With the latter detector noise level and the previously indicated 1.0 μV electronics noise level, electronics noise can contribute an additional 35 percent to the system rms noise level over the 97.6 kHz bandwidth. Note that much of the electronics noise is high frequency and may not impact system MRT, where:

N_E = rms electronics noise voltage referenced to preamplifier input

N_D = rms detector noise voltage referenced to preamplifier input

$$= \frac{R\ (V/W) \cdot 10^6 \cdot [A_d\ (cm)^2]^{1/2} \cdot \Delta f_d^{1/2}}{D^*\ (cm \cdot Hz^{1/2} \cdot /W)} . \qquad \text{(E-17)}$$

One way to express electronics noise to allow ready system performance evaluation is to convert it into an equivalent ΔT for inclusion into the system NEΔT expression. A relationship can be derived by expressing electronics noise as a fraction of the detector noise equivalent ΔT for the system, or:

$$NE\Delta T_{elec} = \frac{N_E\ (\mu V)}{N_D\ (\mu V)} \cdot NE\Delta T_{det} \qquad \text{(E-18)}$$

Substituting Equations (E-17) and (E-4) into Equation (E-18), it is seen that:

$$NE\Delta T_{elec} = \frac{N_E(\mu V)}{\left(\frac{R \cdot 10^6 \cdot A_d^{1/2} \cdot \Delta f_d^{1/2}}{D^*}\right)} \cdot \frac{4 \cdot F\#^2 \cdot \Delta f_d^{1/2}}{\pi \cdot A_d^{1/2} \cdot T_o \cdot T_a\ (5.59 \times 10^{-5})\ D_p^*}$$

$$= \frac{N_E\ (\mu V)}{R(V/W)} \cdot \frac{F\#^2}{T_o \cdot T_a \cdot A_D} \cdot 2.28 \times 10^{-2}\ (°C) \qquad \text{(E-19)}$$

or since $A_d = 2.58 \times 10^{-5}$ cm^2

$$NE\Delta T_{elec} = \frac{N_E\ (\mu V)}{R(V/W)} \cdot \frac{F\#^2}{T_o \cdot T_a} \cdot 8.84 \times 10^2\ (^\circ C) \qquad \text{(E-20)}$$

As an example, when the above electronics noise voltage (1.0 μV) is converted to an equivalent ΔT with F# = 2, $T_o = 1$, $T_a = 1$, and $R = 3.8 \times 10^4$ (V/W):

$$NE\Delta T_{elec} = 0.09^\circ C.$$

The electrical noise, N_E, can be computed from the relation:

$$N_E = \left[\int_o^\infty S_E(f) \cdot H^2_{elec}(f) \cdot df \right]^{1/2} \qquad \text{(E-21)}$$

$$= \left[S_E(f_o) \int_o^\infty S_e(f) \cdot H^2_{elec}(f) \cdot df \right]^{1/2} \qquad \text{(E-22)}$$

$$= \left[S_E(f_o) \cdot \Delta f_e \right]^{1/2} \qquad \text{(E-23)}$$

where

$$\Delta f_e = \int_o^\infty S_e(f) \cdot H^2_{elec}(f) \cdot df \qquad \text{(E-24)}$$

and

$$S_e(f) = \frac{S_E(f)}{S_E(f_o)}$$

where

$S_E(f)$ = processing electronics noise power spectrum (μV^2/Hz) determined from all noise sources occurring after the detector. This spectrum includes module contributions from such sources as the power supply and electromagnetic interference (EMI). These noise sources are included in N_E by referencing them to the preamplifier input. The information for computing common module contributions is provided in Appendix B.

As an alternate method to Equation (E-17), the electronics noise can be included in the Ratches' model by appropriately modifying the detector noise spectrum to include electronics noise. This spectrum must then be renormalized and the detector D* value modified to include the extra electronics noise level.